Organic Transistors Prepared by Self-Assembly and Printing Processes

by

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1 Introduction

Flexible and lightweight electronics realized on large areas has gained considerable attention in recent years [1.1,1.2]. The interest is particularly generated by the increasing demand in low cost large area displays [1.3-1.5], smart cards [1.6-1.8] and radio frequency identification tags (RFID) [1.8-1.10] and the like.

Such electronic devices can only be realized at low cost if novel material systems and new ways of fabricating the devices and systems are developed. Only the combination of theses approaches allow for the realization of flexible and lightweight systems at low or very low cost. Organic semiconductors are a very promising material system used for such applications [1.2,1.6,1.11,1.12]. Organic materials and organic devices can be printed, which allows for large area processing at low fabrication cost.

In this thesis organic thin film transistors (TFTs) will be investigated, which are key elements of organic electronic devices like RFID tags, flexible display media and smart tags. Organic materials like pentacene will be investigated as active materials in thin film transistors. The electrodes of the transistors will be fabricated by microcontact printing. Microcontact printing is one of the most promising printing techniques developed in recent years. Microcontact printing is a method in which a self-assembled monolayer is used to functionalize, modify or pattern surfaces or films. In this thesis microcontact printing based methods are used to pattern metallic electrodes of organic thin transistors.

An introduction to microcontact printing will be given in chapter 2. Different patterning approaches based on microcontact printing are investigated in chapter 3 and 4. Chapter 5 provides an introduction to organic thin film transistors. The chapter describes the fabrication and characterization of organic thin film transistor. The performance of the pentacene thin film transistors with printed electrodes is described in chapter 6. The performance will be compared to OTFTs fabricated by the standard photolithography method.

In order to realize organic integrated circuits or drivers for display applications the thin film transistors have to be electrically stable. The influence of environmental conditions on the pentacene TFTs is investigated in chapter 7. The electrical stability of pentacene TFTs upon prolonged operation is investigated in chapter 8. Finally, a summary of the thesis is given in chapter 9.

References

2 Micro Contact Printing

2.1 Introduction

Patterning of micro and nanostructures is central to modern science and technology, and it is particularly and widely recognized as one of the enabling methods and cornerstones for the revolution of microelectronics. Patterning technologies can be distinguished in either photolithographic (standard) or non-photolithographic (alternative) methods. Photolithography is by far the most common and standard patterning method used in electronics industry [2.1]. However, photolithography is an expensive technology, and it is not necessarily the most suitable technique for all electronic and photonic applications, where micro and nanostructuring is required. For example, standard photolithography is not compatible with organic semiconducting materials [2.2], since the exposure to ultraviolet light and the use of organic solvents may degrade the functional property of the organic materials. Furthermore, optical lithography is not applicable to curved or flexible substrates. Due to these drawbacks a number of alternative micro- and nano- patterning methods, like printing, stamping or embossing have been developed. Of these methods, printing processes have received particular attention, since printing processes allow for patterning of large area and flexible substrates at low cost. The thesis will focus on a printing technique called microcontact printing. Microcontact printing allows for the fast patterning of micro and nano structures over relatively large areas and flexible substrate at low cost.

An introduction to microcontact printing will be given in this section 2.2 of this chapter. In section 2.3, molecular self-assembly processes will be introduced. The section will focus on the formation of self-assembled monolayers, which can be patterned by microcontact printing. The self-assembled monolayers allow for the modification and patterning of surfaces. Finally, the chapter will be summarized in section 2.4.

2.2 The Microcontact printing process

Microcontact printing ($\mu$CP) belongs to the group of “soft lithography” methods. Soft lithography refers to a set of methods that facilitate the fabrication or replication of structures by using elastomeric stamps or molds [2.3]. Microcontact printing is considered as the most frequently used and versatile alternative patterning method of all soft lithographic methods. The method was developed by Kumar and Whitsides at Harvard University in 1993 [2.4]. The method involves the transfer of an “ink” of molecules over a substrate using an elastomeric stamp. The stamp is prepared by the casting an elastomer against a master that has a relief structures on its surface. During the printing process, the “ink” or solution of molecules forms a self-assembled monolayer (SAM) on the substrate. The fabrication of the stamp and the actual stamping process is illustrated in Fig. 2.1

At first microcontact printing was used to print thiol based self-assembled monolayers on metal surfaces [2.4]. The thiol self-assembled monolayer acts as etch resist, so that the underlying metal film can be patterned by wet chemical etching. Later on, microcontact printing has been applied to various materials, including biological molecules [2.5-2.9].
Fig. 2.1: Schematic procedure of microcontact printing (µCP) of a self-assembled monolayer (SAM) on a substrate. The dimensions and the aspect ratio of the stamp are controlled by the relief height (h) and the width (l), and the distance between the features (d).

Presently, the method is considered as one of the enabling technologies to pattern different materials on large area or flexible substrates. So far structures down to 35 nm have been patterned by this method [2.4]. The printed SAMs can be used as a etch mask or a template for selective wetting or selective growth processes. Such approaches allow for the patterning of micro- and nanostructures over a variety of substrates.

Before printing the self-assembled molecules onto the substrates the master and the stamp have to be fabricated. In the following, the fabrication of the master and the stamp will be described before explaining the actual microcontact printing process.

Realization of the master

In the first step the master has to be realized. The master can be fabricated by using optical lithography or electron beam lithography. For fast prototyping, a transparency mask can be used, which exhibits a resolution of 10-20 µm. Electron beam lithography is needed to achieve sub micrometer resolution.

Masters are realized by patterning an epoxy resists over a smooth surface (e.g. silicon wafers or glass substrates). Photodefinable epoxy resists like SU-8 [2.10] allow for the fabrication of structures with high aspect ratios. In order to realize masters with smaller aspect ratios the epoxy resist is replaced by conventional photoresists.
Realization of the stamp

In the second step, the elastomeric stamp is fabricated. The most common elastomer used for the fabrication of the stamp is PDMS (polymethylmethacrylate, \((\text{C}_2\text{H}_6\text{OSi})_n\)). The actual PDMS stamp is fabricated from a mixture of polymer and a cross-linking agent (10:1). The stamp is fabricated by pouring the elastomeric material over the master followed by a curing step. The PDMS is cured for two hours at a curing temperature of 70 °C. A schematic cross section of the elastomeric master and stamp (negative replica of the master) is shown in Fig. 2.1. After curing, the flexible PDMS stamp can be used to print SAMs on different surfaces. The important parameters of the stamp are the relief height \((h)\) and the width \((l)\), and the spacing between the features \((d)\). The aspect ratio of the stamp is determined by the relief height divided by the spacing between the features \((h/l)\). When printing the self-assembled monolayers on the substrate the PDMS stamp forms a conformal contact with the substrate. The PDMS surface has a low interfacial free energy \((2 \cdot 10^{-4} \text{N/cm})\) and good chemical stability [2.11]. Most molecules or polymers being patterned or molded do not adhere irreversibly to, or react with, the surface of PDMS. Besides, PDMS has a good thermal stability (up to 186 °C in air) [2.11], which allows for processing at elevated temperatures. PDMS is a durable material, and the stamp can be used many times (>50) [2.1] to print self-assembled monolayers on rigid or flexible substrates. Furthermore, PDMS is not hydroscopic; so that the material doesn’t swell when it is exposed to humidity [2.1].

The printing process

Finally, as shown in Fig. 2.1, the elastomeric stamp can be used to print molecules onto a substrate. Before printing the molecules onto the substrate, the stamp is “inked” with a solution of molecules (see Table 2.1). In the next step, the PDMS stamp is brought in conformal contact with the surface and the molecules (SAMs) are transferred directly from the stamp to the surface. This process takes only a few seconds and (almost) no pressure has to be applied to the stamp. The transfer process of the molecules and the bonding of the SAMs on the substrate depend on the chemistry of the molecules and the substrate.

2.3 Molecular self-assembly processes

Self-assembly is a strategy for the assembly of molecules or monolayer. The term “self-assembly” was first introduced in 1993 in a report describing the chemically controlled layer-by-layer self-assembly of molecular films [2.12].

A monolayer is formed due to strong molecular-substrate interactions. The process is self-limiting. The self-assembly process stops when all active sites on the surface are occupied by molecules. The SAMs can be transferred from the solution to the substrate either by microcontact printing, dip coating or vapor phase deposition [2.1-2.3]

The typical structure of a SAMs is depicted in Fig. 2.2. Each molecule is typically composed of two groups: a head group that can form a bond with a substrate and a tail group that modifies the surface physical and chemical property. Often, the molecules
also contain functional end group, which allows for further physical or chemical functionalization of the molecules.

Only molecules with defined functional head groups can be attached to specific surfaces. The chemistry of the head group of the molecules and the substrate has to be matched. Furthermore, before printing or depositing the molecules onto the surface the substrate should be very clean. Despite such limitations self-assembly processes are widely used to modify surfaces. Self-assembled monolayers are extremely stable, mechanically strong, uniform, and ultra thin. Some SAMs are even stable at elevated temperature up to 400 °C [2.13].

However, in some cases the SAMs has to be removed from the surface as part of the patterning process. SAMs can be removed from the surface by an oxygen plasma or reactive ion etching [2.14], ultraviolet (UV) ozone treatment [2.15], elevated heat treatment (e.g., above 400 °C) [2.16] or using a beam of neutral atoms [2.17].

The self-assembled monolayers used in this thesis were removed by an ultraviolet (UV) ozone treatment. Exposing the sample to UV light leads to the formation of molecular oxygen and ozone (O$_3$). The ozone and oxygen again activated by the UV light will attack the organic contamination (SAMs) and removes it from the substrate as small volatile molecules like CO$_2$, H$_2$O, and the like.

**Fig. 2.2: Formation of self-assembled monolayers on a surface. The molecules forming a self-assembled monolayer consist of head, tail and end groups.**

Within the last decades self-assembled monolayers have found several applications in material science, electronics, photonics, biochemistry, biophysics and the like. The basic reason for using SAMs relies on controlling the surface chemistry of a material independently from the bulk properties of the material. The most commonly used applications of self-assembled monolayers are listed in the following:

**Etch resist:** Depending on the type of the SAM, the monolayer can be used as a etch resist, which allows for patterning of substrates.

For example: Alkene thiols on a gold surface can be used as resist. The uncovered areas can be etched away by a cyanide solution. Similarly alkyl phosphonic SAMs, R-PO$_3$H$_2$, have been used as etch resist to pattern ITO and IZO [2.18].

**Surface modifier:** Self-assembled monolayers can be used to functionalize surfaces.
The surface modification can be applied over the entire surface by dip coating or evaporation methods. Alternatively the self-assembled monolayers can be formed selectively by microcontact printing processes.

For example: Silane based self-assembled monolayers can be used to form hydrophobic areas on silicon or glass substrates.

**Selective deposition process:** Patterned SAMs can be used as template to control site selective deposition by creating a heterogeneous nucleation site, or site selective reactions over a substrate. The selective deposition has been demonstrated for physical and chemical vapor deposition processes.

**Selective wetting process:** Patterned SAMs can be used as template to control the wetting processes of surfaces.

For example: Patterned SAMs have been used for selective wetting or dewetting of different fluids or polymers.

**Sticking and anti-sticking layer:** The adhesion properties of materials can be controlled by self-assembled monolayers. Different SAMs have been used to improve or prevent the adhesion of different materials.

A summary of the organic molecules used for self-assembly processes is given in Tab. 2.1. The materials are listed with the corresponding matching substrates. In the following the thesis will mainly focus on silane and thiol SAMs.

<table>
<thead>
<tr>
<th>Self Assembled Monolayer</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Organosilicon (silane) derivatives (e.g., R-SiCl₃)</td>
<td>SiO₂, Al₂O₃ (hydroxilated surfaces) glass, quartz</td>
</tr>
<tr>
<td>Alkane thiols (R-SH)</td>
<td>Gold, silver, palladium and copper</td>
</tr>
<tr>
<td>Dialkyl sulfides (R-S-R, R-S-S-R)</td>
<td>Gold</td>
</tr>
<tr>
<td>Carboxylic acids (R-COOH)</td>
<td>Aluminum oxide and silver</td>
</tr>
<tr>
<td>Phosphonic acid (RPO₃H₂)</td>
<td>Aluminum oxide, In₂O₃/SnO₂ (ITO),</td>
</tr>
<tr>
<td>Carboxylic (R-COOH) and Hydroxamic (RCONHOH) acids</td>
<td>Metal oxides</td>
</tr>
</tbody>
</table>

*Tab.2.1: List of materials, which can be used as self-assembled monolayers and corresponding substrates. R-represents a radical (CₙH₂n+1 ) group [2.1].*

### 2.3.1 Silane self-assembled monolayers

Silanes (SiₙH₂n+2) based self-assembled monolayers are the most commonly used self-assembled monolayers. Such monolayers are adsorbed onto hydroxylated surfaces like silicon dioxide or glass. SAMs like octadecyltrichlorosilane (OTS, CH₃(CH₂)₁₇SiCl₃) bind
to the surface hydroxyl groups via the formation of silicon-oxygen bonds. The head group of the molecules contains chlorosilane groups, which in the presence of water liberate the chlorine atoms and form hydroxyl groups, Si-OH (silanol) as shown on Fig. 2.3.

Next, these groups, which are strongly attracted to the hydrophilic silicon dioxide surfaces, condense and react with silanols on the precursor molecules and the silanols on the surface produce covalent siloxane bonds, Si-O-Si. The condensation of a monolayer takes several minutes up to several hours depending on the concentration of molecules in the solution. The complete polymerization of silanols into a covalent siloxane network requires aging of the surfaces in air for a few days or baking at 100 °C – 120 °C for a few days [2.18].

Fig. 2.3: Formation of an octadecyltrichlorosilane (OTS) based self-assembled monolayer on a silicon oxide surface.

In order to form a silane based self-assembled monolayer, several steps have to be taken into account. Firstly, the silicon wafers have to be cleaned by a piranha solution (H_2SO_4: H_2O_2 with 4:1) for about 30 minutes. After the piranha is washed away with distilled water, the wafer is dried and used immediately for µCP of OTS.

Several studies indicate that water near the substrate or humidity has a strong influence on the monolayer formation. OH-groups have to be present on the substrate; otherwise no SAM can be formed [2.19].

On a fully hydroxylated oxide surface, the density of OH groups is approximately 1 per 20 Å², which is close to the packing density of OTS [2.16]. However, these OH groups are randomly arranged and therefore it seems unlikely that each OTS molecule could
individually bind to the substrate. Instead, neighbouring molecules cross-link to each other to form complete monolayers [2.20].

The deposition of SAMs like OTS onto an OH-terminated surface leads to a significant change of the surface energies of the substrate. Areas covered by OTS turn hydrophobic, whereas untreated areas are hydrophilic. The difference in surface energy can be used to selectively pattern or selective growth of materials on a substrate. To characterize the treated surfaces water contact angle measurement are often used.

2.3.2 Thiol self-assembled monolayers

In 1983 Allara and Nuzzo reported the formation of SAMs from organic disulphides on gold films [2.21]. Their work initiated a lot of research on thiol SAMs since the process could be potentially used to pattern metal film and replace conventional optical lithography approaches. Thiol SAMs can easily be patterned over coinage metals by a printing process. The formation of a thiol SAMs on a gold surface is shown in Fig. 2.4. Thiol SAMs can also be patterned over other coinage metals like silver, copper, and palladium in the same way.

![Thiol SAM diagram](image)

Fig. 2.4: Formation of an eicosanethiol (ECT) based self-assembled monolayer on a gold surface. Thiol SAMs can also be patterned over other coinage metals like silver, copper, and palladium in the same way.

Structurally the thiol based SAM consists of a SH-head group, and a tail group, which can be formed by a radical \((C_nH_{2n+1})\) or an organic benzene derivative. Many families of thiol SAMs include hexadecanethiol (HDT, \(CH_3(CH_2)_{15}SH\)), octadecanethiol (ODT, \(CH_3(CH_2)_{17}SH\)), eicosanethiol (ECT, \(CH_3(CH_2)_{19}SH\)). Thiol SAMs with radical group are typically used as etch resists or etch masks. Metal films, e.g. gold, can be patterned by using an alkyl thiol SAM etch resist and a ferri/ferrocyanide etchant. Such approach can be used in the fabrication of electrodes for the realization of organic electronics. However, it is important to note that thiol SAMs are no compatible with standard gold etching solutions like potassium iodide/iodine solution \((KI/I_2)\). Furthermore, the ferri/ferrocyanide etching solution is not environmental friendly. A more detailed description on the patterning process using thiol SAMS will be given in chapter 4.
Furthermore, thiol based SAMs can be used to modify the surface wetting properties of metallic films. For example Benzene derivatives of thiol SAMs like thiophenol (TP), 4-nitrothiophenol (4-NTP), and 2-mercapto 5-nitrobenzimidzole (MNB) are typically used to modify the properties of metal electrodes. A more detailed description will be given in chapter 6.

2.4 Summary

Microcontact printing of SAMs is a versatile technique that can be used in patterning surfaces with ultra thin molecular layers. Microcontact printing allows for patterning of micro- and nano- structures over flexible or rigid substrates. Soft stamps are used to transfer and pattern self-assembled monolayers onto a variety of substrate. Printing of silane based SAMs on a matching substrate like silicon substrate or glass lead to the formation of hydrophobic areas on the substrate, whereas the unexposed areas stay hydrophilic. The combination of the method with other techniques like a selective wetting process allows for patterning of a variety of materials. Printing of thiol based SAMs on substrates like silver or gold lead to the formation of hydrophobic areas on the substrate, whereas the unexposed areas stay. Furthermore, the patterned thiols can be used as etch mask or etch resist. Details on patterning materials by using microcontact printed silane and thiol SAMS are described in chapter 3 and 4.

References

3 Printing of Silane Self-Assembled Monolayers

3.1 Introduction

Many novel and alternative patterning technologies have been developed in recent years to realize micro and nano structures over large areas. Of the alternative methods, microcontact printing has gained considerable attention. The method facilitates the patterning of materials on large areas and curved substrates at relatively low cost. Therefore, microcontact printing has become a widely used technique in organic and large area electronics, biochemistry, and material science [3.1,3.2].

During the printing process, a self-assembled monolayer (SAM) is transferred from a stamp to a rigid or flexible substrate. The SAM forms bonds with the substrate or chemically modifies the surfaces of the substrate. The printed monolayer or SAM can be used as a resist. To date, gold [3.3-3.5], silver [3.6], copper [3.7,3.8] metal films have been patterned using thiol SAMs as etch resist. Similarly, efforts have been made to pattern materials like silicon [3.9-3.12], silicon dioxide [3.12], and glass [3.13] using alkyl silane SAMs as etch resist. Furthermore, printed SAMs can be used as a template to control selective growth of organic and inorganic materials on different substrates [3.14,3.15] or to guide site-selective wetting or electropolymerization [3.16,3.17].

The use of self-assembled monolayers as templates for selective wetting is described in this chapter. Microcontact printing in combination with selective dewetting is a generic approach that allows for patterning of conductive polymers, semiconductive polymers, and resists [3.18-3.20]. For example, conductive and semiconductive polymers were patterned by selective wetting in order to realize organic thin-film transistors [3.19,3.20]. Furthermore, selective wetting was used to pattern prepolymer. Subsequently, the prepolymer were used as an etch mask to pattern silicon substrates by wet-chemical etching [3.17,3.18].

In this chapter the patterned prepolymer is used to lift-off different metallic structures like micro-coils, interconnects, and electrodes. The microcontact printing and selective dewetting process is described in section 3.2. Experimental results are presented in section 3.3. In section 3.4 the influence of the printing and selective-wetting process on the achievable resolution is discussed. Furthermore, wetting of homogeneous and heterogeneous surfaces will be compared to study the underlying physical limitations of the selective-wetting process (section 3.5). Finally, a summary of the chapter is given in section 3.6.

3.2 Microcontact printing of silane self-assembled monolayers

During the printing process of self-assembled monolayers, an elastomeric stamp is brought in conformal contact with the flexible or rigid substrate. The stamps were prepared by casting an elastomeric material such as polydimethylsiloxane (PDMS) against a relief structure (master). Afterwards, the elastomer was cured and removed from the master.
Fig. 3.1: Micrograph of an optical mask (a) which was used to prepare a master based on an epoxy resist (SU-8) (b). Magnified micrograph of the master is shown in (c). The bright regions are the silicon substrate and the dark regions correspond to the SU-8 resist. A micrograph of a stamp (negative replica of the master) is shown in (d).

The masters were fabricated by using optical lithography. Masters were realized with aspect ratios ranging from 1.5 to 7. Fig. 3.1 shows micrographs of the mask (a), master (b,c) and the PDMS stamp (d) used for the printing process. An epoxy-based resist [3.21] was used to realize structures with high aspect ratios.

In the next step, the stamp was coated by a SAM. In this study, octadecyltrichlorosilane (CH$_3$(CH$_2$)$_{17}$SiCl$_3$), or OTS, was used as a SAM. The OTS molecules were dissolved in hexadecane before coating the stamp. The OTS molecules consist of a long-chain alkyl group (C$_{18}$H$_{37}$) and a polar head group (SiCl$_3$). The head group of OTS forms a Si-O-Si bond to SiO$_2$ or glass substrates when printed on the substrate.

Before printing the monolayers on the glass or silicon substrates, the surface of the wafers were terminated by OH groups using a mixture of sulfuric acid (H$_2$SO$_4$) and hydrogen peroxide (H$_2$O$_2$). Water contact angle measurements were used to characterize the surface properties of the substrates. An “out-of-the-box” silicon wafer exhibits a contact angle of 28°-32° (see Fig. 3.2a). The cleaning procedure leads to the formation of a hydrophilic surface, i.e., complete wetting and spreading of water droplets on the silicon surface was observed. Transferring the OTS molecules to silicon or glass substrate leads to the modification of the surface energies. The exposed areas turn hydrophobic, whereas the unexposed areas remain hydrophilic.
Fig. 3.2: Micrographs of water droplets on “out-of-the-box” and octadecyltrichlorosilane (OTS) treated silicon wafers. The “out-of-the-box” silicon wafer exhibits a contact angle of 28°-32°, whereas the printed octadecyltrichlorosilane exhibits a contact angle of 93°–115°.

The hydrophobic areas are formed by creating a bond between the Si head group of OTS and the substrate. The hydrophobic areas exhibited contact angles in the range of 90°-113° (see Fig. 3.2b). A comparison of the printed SAMs with spin-coated OTS exhibits similar contact angles of 93°–115°. Both measurements are in good agreement with measurements in literature [3.22].

3.3 Selective surface wetting

After functionalizing the surface with a SAM the substrates were coated with a polymer. The polymers were either dip or spin coated. The polymers form a film in the hydrophilic regions of the substrate, whereas the hydrophobic regions stay uncoated. The selective dewetting/wetting process is illustrated in Fig. 3.3a. Resists like polymethyl methacrylate, PMMA, and polymers like prepolymer polyurethane, and PEDOT-PSS (poly(3,4-ethylenedioxythiophene) - polystyrenesulfonate) were selectively deposited on the substrate. The resolution of the selective wetting process is determined by the viscosity of the polymer, the surface tension of the substrate and the spinning or dipping conditions. Micrographs of a PMMA resist pattern, PEDOT-PSS and prepolymer polyurethane are shown in Fig. 3.4. The highest resolution was achieved for the prepolymer polyurethane. Features down to 1 µm could be patterned by using this material combination. Finally the OTS monolayers were removed from the substrate by a UV/ozone treatment. The polymer pattern on the substrate can now be used to further process the sample.

The patterning approach described here is a universal patterning process that facilitates patterning of a variety of materials. Conductive polymers like PEDOT-PSS (poly(3,4-ethylenedioxythiophene) - polystyrenesulfonate) can be used as electrodes in organic electronics. Prepolymer like polyurethane can be applied as insulators. However, in the following the resist/PMMA patterns will be used to pattern metal films like gold, tungsten, and titanium films by a lift-off process. The patterned resist/PMMA structures on the substrate are comparable to resist patterns generated by optical or e-beam lithography.
3.4 Patterning of metal structures

In the following the process was used to realize radio-frequency (RF) micro-coils, electrical interconnects, and electrodes for organic field-effect transistors (OTFTs). Since microcoils and electrodes for organic thin film transistors can be realized at the same time on the process is perfectly suitable for fabricating radio frequency identification tags (RFID tags) or other electronic and photonic devices on rigid or flexible substrates. The process flow of patterning metal electrodes is described in Fig. 3.3b.

Micrographs of an elastomeric PDMS stamp used for fabricating micro-coils are shown in Figs. 3.5a and 3.6b. The stamp was used to print the SAMs on silicon wafers. After the printing step, the substrates were dip-coated in diluted PMMA. A micrograph of a patterned PMMA film is shown in Fig. 3.5c. Windings of a printed micro-coil can be seen in Fig. 3.5d. After forming the PMMA pattern on the substrate, the OTS was removed by an ozone treatment. The windings have a width and spacing of 50 µm. Coils with dimensions ranging from 20 to 200 µm were realized.

The micro-coils were realized by depositing gold on the pre-patterned substrates. To improve adhesion of the gold film on the substrate, a 3-5 nm-thick titanium film was prepared prior to depositing gold. In the next step, the undesired areas were lifted off. Gold was used for this experiment because it exhibits high conductivity and high work function, which facilitates the realization of coils with high quality factors (Q-factors), and electrodes for organic devices such as thin-film transistors.
Fig. 3.4: Polymer films patterned by selective wetting: (a) PMMA on silicon substrate; (b) PEDOT/PSS pattern (conductive polymer) on silicon substrate; and (c) prepolymer polyurethane on silicon substrate.

Impedance measurements of the micro-coils on glass and silicon wafers exhibit results comparable to coils patterned by standard photolithography. The coils exhibit an inductance of about 1 μH, which is comparable to standard coils used for RFID tags that operate at 13.56 MHz [3.23].

Fig. 3.5: Micrographs of a micro coil pattern on a PDMS stamp (a), magnified image of the PDMS stamp (b), patterned polymer on silicon substrate (the dark region exhibits PMMA resist, and the bright region shows the silicon substrate covered by OTS) (c), and patterned metal film (Au/Ti) on a silicon substrate (d).
In addition to the coils, electrical interconnects and electrodes for organic transistors were realized. The smallest structures prepared on OTS-treated silicon substrates using selective wetting of PMMA exhibit a dimension of 2 \( \mu m \). The smallest dimension is used to define the channel length of an organic thin-film transistor. A micrograph of the electrodes (drain and source electrodes) with a spacing of 5 \( \mu m \), 10 \( \mu m \) and 20 \( \mu m \) are shown in Fig. 3.6. For the 2 \( \mu m \) structures, the edges of the electrodes begin to become fuzzy, which prevents the reproducible fabrication of organic transistors.

![Image of electrodes with different gaps](image)

**Fig. 3.6:** Gold electrodes patterned by a combination of selective wetting and a lift-off process. Electrodes with gaps of 20 \( \mu m \) (left), 10 \( \mu m \) (middle), and 5 \( \mu m \) (right) were realized.

### 3.5 Factors influencing the patterning process

The resolution of the patterning process depends on several parameters such as the microcontact printing, surface energies of the heterogeneous substrate, geometry of the features, viscosity of the resist/polymer, and capillary forces. Furthermore, the resolution of the selective-wetting process is affected by the inclination angle between the substrate and reservoir of resist and the speed of withdrawal. In the following, the individual aspects will be discussed in terms of fundamental limitations of the process and achievable resolution.

#### 3.5.1 The printing process

In general, the patterning approach described here is limited by the selective-wetting process, rather than the microcontact printing process, because it is possible to achieve sub-100 nm structures by microcontact printing [3.2,3.5]. Nevertheless, the fabrication process and the resolution of the patterned features are influenced by the printing of the SAM, which is again influenced by the master and PDMS stamp. The aspect ratio of the PDMS stamp strongly influences the printed features. Using an epoxy resist to prepare the master results in high aspect ratios of 5-15 because the epoxy film is typically relatively thick (10-30 \( \mu m \)). Such high aspect ratios are of particular interest if the packing density of the printed structures is relatively low. Otherwise, sagging of the PDMS stamp occurs because of comprehensive force between the stamp and the substrate. This effect distorts the printed features. To achieve the minimum possible feature size, the aspect ratio must be reduced. The smallest features were printed using stamps with aspect ratios less than 1.5. Three factors were identified which limit the resolution of the microcontact printing process. For high aspect ratios, pairing of the elastomer is observed. On the other hand, for low densely packed structures, sagging of the elastomer occurs. The possible structural defects that can arise from the different
aspect ratio of the stamp are schematically represented in Fig. 3.8. Both problems limit the resolution of the microcontact printing process. Reducing the aspect ratio of the relief structures, redesigning or optimizing the geometries of the structures can minimize the problem. The aspect ratio of the stamp can also be controlled by varying the PDMS cross-linking agent ratio. Thus, decreasing the concentration of the PDMS can partially reduce mainly the sagging problem. Furthermore, the use of a rigid backplane over the master can alleviate such problems [3.24].

On the other hand, for high aspect ratios structure the microcontact printing process is limited by the sidewall formation of the masters. If the sidewalls of the master are not perfectly vertical, the dimensions of the printed features may deviate from the initial features. As a consequence, delamination of the PDMS structures from the stamp occurs. The situation can be improved by modifying the exposure conditions while preparing the master [3.25].

![Fig. 3.8: Schematic cross section of PDMS stamp of different dimensions: Ideal structure (a), Lateral collapse observed for h>>d (b), collapse for h>>d (c) and sagging for d>>h (d).](image)

3.5.2 The wetting process

Selective wetting is a promising technique to pattern conductive polymers or resists. The approach is of particular interest to organic electronics because several materials are sensitive to solvents, which prevents the patterning of organic films by standard semiconductor processing. Selective wetting/dewetting of polymers or resists can be achieved if the surface of the substrate is pre-patterned [3.19,3.20]. In this study, we used OTS, which forms regions of low surface energy (hydrophobic) on glass or oxidized silicon wafers. To increase the selectivity between the different regions of the heterogeneous substrate, the surface energies of the substrate can be maximized by cleaning the substrate in a mixture of sulfuric acid and hydrogen peroxide.

Different techniques can be applied to coat the heterogeneous substrate by a polymer or a resist. The polymer can be inkjet-printed [3.21], the substrate can be dip-casted, or the polymer can be spin-coated on the substrate. Inkjet-printing is a serial process, whereas dip-coating and spin-coating are parallel process, which are more suitable for large-area processing. Therefore, we concentrated in this study on dip-coating.
A.) Dip-coating of homogenous surfaces

Before discussing the selective wetting/dewetting of polymers on heterogeneous substrates, the wetting of polymers on homogenous substrates will be discussed. The formation of a polymer film after dipping a homogeneous substrate in a reservoir of a Newtonian liquid was first described by Laudeau et al. [3.26] and Deryagin and Levi [3.27]. They assumed in their studies that the gravitational forces of the liquid are negligible and that a balance between viscosity and capillary forces determines the thickness of the film (see Fig. 3.9). In this case, the entrained film thickness is given by

\[ h_o \propto l_c \cdot Ca^{3/2} \]  

(3.1)

where \( Ca \) is the capillary constant, which is calculated by \( Ca = \mu U / \sigma \) (see Fig. 3.9). Here, \( \mu \) is the viscosity of the polymer, \( U \) is the withdrawal speed of the substrate out of the polymer reservoir, and \( \sigma \) is the surface tension of the substrate. The parameter \( l_c \) in Eq. (3.1) is the characteristic length, given by \( l_c = \sqrt{\sigma/2 \rho g} \). The characteristic length is calculated by \( \sigma \), the surface tension of the homogenous surface; \( \rho \), the density of the polymer; and \( g \), the gravitational constant. The characteristic length represents the radius of curvature of a static capillary meniscus. It is assumed in Eq. (3.1) that the substrate is withdrawn from the reservoir using an inclination angle, \( \alpha \), of 0°. The inclination angle is defined as the angle between the surface normal and substrate. To describe the withdrawal of the substrate from the reservoir under certain inclination angles, the withdrawal speed \( U \) in Eq. (3.1) must be replaced by \( U / \cos \alpha \).

\[ h_o \propto l_c \cdot Ca^{3/2} \]  

(3.1)

Eq. (3.1) describes the height of the polymer film if an infinitely extended substrate is dip-coated. The same equation even applies to a heterogeneous substrate if the patterned areas on the substrate are large in comparison to the height of the film.
B.) Dip-coating of heterogeneous surfaces

For heterogeneous surfaces, the situation gets significantly more complex, even though the underlying theory remains the same. To achieve a thermodynamic equilibrium, the total energy of the system must be minimized. The total energy of the system is given by the sum of the kinetic and potential energies. The kinetic energy is a function of the flow of the polymer, which depends on the speed of withdrawal, \( U \); the viscosity of the polymer; \( \mu \), and the height of the film, \( h \). The interfacial potential energy is defined by three energies at the interface between solid-liquid, liquid-vapor, and solid-vapor (\( \gamma_{sl} \), \( \gamma_{lv} \), and \( \gamma_{sv} \), respectively). Hence, the minimum potential energy is controlled by these parameters.

![Diagram](image)

**Fig. 3.10:** Schematic top (a) and cross section (b) of a polymer pattern on a pre-patterned substrate.

Several theoretical studies have been published in recent years describing the wetting of heterogeneous substrates [3.28, 3.29]. To simplify the problem Darhuber and coworkers concentrated on the steady-state entrainment of a liquid on a single hydrophilic strip surrounded by a hydrophobic coating [3.30]. Such a structure is illustrated in Fig. 3.10. For such geometries, which are very similar to our electrodes, coils, and interconnects; the following expression for the entrained film height can be derived,

\[
h_w \approx W \cdot Ca^{\frac{1}{3}}
\]

where \( W \) is the half-width of the hydrophilic strip. They derived the expression by using the Navier-Stokes equation describing the steady-state flow of a liquid. The equation was derived assuming that the capillary number is much smaller than 1 (\( Ca << 1 \)). Furthermore, it was assumed that the angle between the flow direction of polymer and the hydrophilic strip is zero. Comparing Eq. (3.1) and Eq. (3.2) indicates that the
exponent of Ca is decreased from 2/3 to 1/3. Furthermore, the length scale controlling the deposited film is not the capillary length, but the half-width of the hydrophilic strip.

If the width $W$ of a strip is much larger than the critical length $l_c$, the maximum height of the film is described by Eq. (3.1). If the width of a strip is in the range of the critical length, the maximum height is described by Eq. (3.2). Under such conditions, the resist forms an arc-like structure, as shown in Fig. 3.10. Eq. (3.2) reveals that the height is proportional to the width of the structure. With decreasing width the height of the features is reduced. This was experimentally confirmed.

![Graph showing measured height profile of a polymethylmethacrylate, PMMA, resist pattern on a silicon substrate.](image)

*Fig. 3.11: Measured height profile of a polymethylmethacrylate, PMMA, resist pattern on a silicon substrate.*

A linear relationship between the width of the strip and the height of the polymer profile can be observed over a wide range. Surface profilometry measurements of resist patterns were carried out to determine the relationship between the height and width of the resist structures. The height of the resist structures for different strips of resist is shown in Fig. 3.11. The experimental results show a linear relationship between height and the width of the resist profile. The experimental results are in a good agreement with the equation 3.2. This experimental finding is consistent with investigations in literature [3.30].

This linear relationship between the height of the film and the width of the strip applies only above certain width of the hydrophilic strip, i.e. dewetting results, if the substrate-polymer interactions are stronger than the polymer-polymer interactions. If the polymer-polymer interactions are stronger than the substrate-polymer interactions, the polymer pattern bulges out and the resist strips cannot be formed on the substrate. This situation occurs for smaller features or high-viscosity resists.
Fig. 3.12: Relationship between the height of a prepolymer PMMA and the width of a resist stripe, which was prepared by selective wetting on a heterogeneous substrate.

To achieve smaller features on the substrate and to increase the resolution of the printing process, the withdrawal speed $U$, viscosity $\mu$, and surface tension $\sigma$ have to be optimized. Decreasing the viscosity of the polymer leads to a reduction of the height of the film. The viscosity of PMMA can be controlled by changing the number of monomers per chain. With a decreasing number of monomers, the viscosity of the resist is decreased. Therefore, PMMA with the lowest available number of monomers was used in our study. To decrease the viscosity, the polymer can be diluted by a solvent. However, further decrease of the viscosity of the polymer does not necessarily lead to higher resolution. The interaction energy between the polymer, substrate, and solvent changes as the solvent concentration is increased. And this can result in nonselective wetting over the substrate, which limits the resolution of the printing process. Besides the viscosity, the height of the film can be reduced by decreasing the withdrawal speed, which scales by $U^{1/3}$. Consequently, the withdrawal speed was reduced to a minimum.

Another important issue in patterning polymers is the thickness of the patterned polymer, where it is a determining factor for lift-off or metallization. Polymers whose viscosity is very low, e.g., by adding a solvent, may be able to pattern low features or high resolution. However, such polymers may result ultra-thin patterned polymer films, it may lead to an in incapability of the polymer film for the lift off process. Such problems can be addressed by selecting a polymer whose selective dewetting is very high and can be patterned with a preferred thickness for low features.

C.) Influence of device geometries

So far, we have discussed the selective wetting of polymers or resists on hydrophilic pre-patterned strips. The angle between the polymer flow-direction and the hydrophilic
strip was assumed to be zero. The situation changes as we move to more complex device geometries such as micro-coils. The resolution of the selective-wetting process increases as the angle between the flow direction of the polymer and the hydrophilic strip increases. If the hydrophilic strip on the substrate is parallel to the polymer flow direction, a minimum feature size of 2 \( \mu \text{m} \) was achieved using PMMA. For spiral-like structures (RF micro-coils), the smallest dimension was increased to 20 \( \mu \text{m} \) for the same material. This is because orthogonal structures are pre-patterned on the substrate. Furthermore, the structures on the substrate are more or less closed (windings of the coil). The closed structures prevent the flow of excess polymer. This leads to bulging and a nonuniform pattern formation of the polymer film.

3.6 Summary

Microcontact printing of self-assembled monolayers in combination with selective dewetting can be used as a universal patterning approach of polymers. The process provides a simple route in patterning conductive or semiconducting polymers, or resist structures. In this chapter self-assembled monolayers like OTS were microcontact-printed on glass or silicon substrates and PMMA resist were selectively patterned on substrates. The patterned resist structures were used to pattern titanium and gold films by a lift-off process. Radio-frequency micro-coils, interconnects, and electrodes for transistors were realized by this approach. The resolution of the process is determined by the selective dewetting of polymers and not by the microcontact-printing of the SAMs. The resolution of the selective-dewetting process depends on several parameters, including the surface tension of the substrate and viscosity of the polymer. A resolution of 2 \( \mu \text{m} \) was achieved for parallel electrodes using a combination of microcontact printing of OTS and selective dewetting of PMMA. Furthermore, the achieved resolution depends on the geometry of the printed structures. For complex structures such as micro-coils, the resolution was reduced to 20 \( \mu \text{m} \). Fundamentally, the resolution of the selective-wetting process is limited by the surface tension of the substrate and viscosity of the polymer, which again depends on the polymer type, solubility of the polymer, and intermolecular forces between the polymer chains and solvents. Generally, this method facilitates a new universal approach in patterning different materials on the micro and nanoscale.

References

4 Printing of Thiol Self-Assembled Monolayers

4.1 Introduction

Microcontact printing (μCP) has become an important technique in patterning micro- and nanostructures. The most popular microcontact printing structuring approach is based on using an alkyl thiol SAMs as etch mask or resist. The approach was introduced by Whitesides and coworkers, who used microcontact printing to define thiol patterns on gold substrates [4.1]. The film was patterned by a ferri/ferrocyanide etching solution after printing a hexadecanethiol (HDT, CH₄(CH₂)₁₅SH) SAMs onto the gold film. Following this study, the HDT SAMs were also applied as etch resist to pattern silver [4.2-4.4], copper [4.5-4.8] and palladium [4.9]. The use of a standard gold etching solutions (e.g., potassium iodide/iodine solution, KI/I₂) is not possible since the thiol SAMs cannot withstand the standard etching solution. The major advantage of using thiol SAMs as etch resist is that the method can be applied to pattern microstructure over large areas. Furthermore, the method is easy to use, and can be applied for different metals (Au, Ag, Cu, and Pd).

However, the method exhibits also some disadvantages. Only thin metal films can be patterned by the method since the etching solution exhibits a relatively poor selectivity between the thiol SAM and the gold film. Furthermore, the etching solution (ferri/ferrocyanide) is not compatible with standard chemicals used in semiconductor processing. Thus, an alternative and environmental friendly approach was developed, which allows for patterning of thicker coinage metals. The approach is based on using a self-assembled thiol monolayers as a selective dewetting agent. However, the patterning process is more complex which limits its application in large area and low cost electronics.

The surface engineering of gold and silver surfaces by thiol SAMs is described in section 4.2. In section 4.3 the thiol self-assembled monolayers were used as etch resist or etch mask. In the section 4.4 the microcontact printed thiol self-assembled monolayers were used as selective wetting agent. Polymers like polymethylmethacrylate (PMMA) were selectively deposited onto the substrate, where they form resist patterns that can be used to pattern the underlying metal film by conventional etching solutions. Finally the results are summarized in section 4.5.

4.2 Surface engineering by printed thiol self-assembled monolayers

A solution of an alkyl thiol SAM was used as “ink” for the surface modification of gold and silver. An elastomeric stamp was used to print the thiol based self-assembled monolayers on silver or gold films. A detailed description of the preparation of the PDMS stamp is described in chapter 2, respectively. The silver and gold films were prepared by electron beam evaporation. To improve the adhesion of gold films on the glass substrates and silicon wafers a 3 nm titanium film was deposited prior the evaporation of the gold and silver metal films.

Prior to microcontact printing the gold and silver surfaces were cleaned by using a NH₄OH solution and ozone treatment, respectively. The resulting substrates were
hydrophilic. Measurements of the contact angle showed complete wetting of water droplets on the cleaned metal surfaces.

The alkyl thiol SAM used to modify the surface of silver and gold films in this study is eicosanethiol, ECT (CH\textsubscript{3}(CH\textsubscript{2})\textsubscript{19}SH). Thiol molecules like CH\textsubscript{3}(CH\textsubscript{2})\textsubscript{19}SH (eicosanethiol, ECT) consist of a radical or alkyl group, which is terminated with a thiol (-SH) group. Before printing the self-assembled molecules on the metal surfaces, the alkyl thiol molecules were spin coated on the PDMS stamp at 1000 rpm for 1 min. The ECT SAM solution was prepared according to Ref. 4.10.

During the printing process, the stamp was brought in conformal contact with the substrate, so that the self-assembled molecules are transferred from the stamp to the substrate in the regions of contact. The head group of the thiol molecules forms a bond with the gold surface, i.e., S-Au bond. After printing, the regions covered by ECT SAMs are hydrophobic, whereas the unexposed regions stay hydrophilic. The surface wetting behaviours of the two regions were characterized by water contact angle measurements. Complete wetting is observed in the hydrophilic areas, whereas the hydrophobic regions exhibit contact angles in the range of 110° -114°.

A schematic cross section of a patterned ECT SAM on a metal surface is shown in Fig. 4.1. The patterned SAMs cause a physicochemical modification of the silver or gold surface. The surface properties of the material are controlled independently from the bulk properties. The presence of the long radical chains allows for used the SAM as etch resist. Alternatively the printed SAM can be used as surface wetting agent.

![Fig. 4.1: Printed eicosanethiol (ECT) SAMs on a silver or gold surface. The patterned SAMs can be used as etch mask or dewetting agent.](image)

Different routes to pattern noble metal by thiol SAM are shown in Fig. 4.2. In Fig. 4.2a, the printed ECT SAM is used as resist mask. The SAM acts as a protection layer while the bare silver or gold regions are etched away by a ferri/ferrocyanide solution. The method allows for patterning of sub 100 nm structures [4.11].

However, the etching solution is not environmental friendly and therefore not compatible with standard chemical used in semiconductor processing. Furthermore, the methods does not allow for patterning of relatively thick metal films (>50nm). Here, it is important to note that standard gold and silver-etching solutions like potassium iodide/iodine (KI/I\textsubscript{2})
cannot be used since the etchant would remove the thiol SAM together with the metal surface, i.e., the etchant is not selective.

An alternative method is described in Fig. 4.2b. Here the patterned SAM is used as a dewetting agent that allows for the selective wetting of a polymer in the uncovered region, whereas the SAM covered region stays uncovered. Consequently, the patterned resist or polymer is used as etch resist, while the bare region is etched by the relatively environmental friendly potassium iodide/iodine (KI/I$_2$) etching solution. The details of the two patterning methods are described in section 4.3 and 4.4.

Fig. 4.2: Patterning of noble metals like silver and gold by microcontact printing of thiol based self-assembled monolayers (SAMs). a.) The thiol based self-assembled monolayer acts as etch mask for silver and gold. The uncoated regions were etched away by a ferri/ferrocyanide solution. b.) The thiol based self-assembled monolayer acts as selective surface wetting agent for a polymer or a resist. The gold or silver films are patterned by a KI/I$_2$ etching solution.

### 4.3 Alkyl thiol self-assembled monolayers as etch resist

The use of alkyl thiol SAMs as etch resist is a low cost method to pattern coinage metals like gold and silver. The method allows for patterning of metal structures over large area and/or flexible substrate.
In the following, a microcontact printed alkyl thiol SAM in combination with a ferri/ferrocyanide etching solution was used to pattern gold and silver films. Micrographs of patterned gold electrodes are shown in Fig. 4.3. The ferri/ferrocyanide etching solution was prepared based on the standard procedure described in Ref. 4.10. Fig. 4.3a shows a 15 nm gold film patterned on a silicon substrate, and Fig. 4.3b shows a 25 nm gold film patterned on a plastic foil. Both structures were etched almost without defect. The time required for the complete etching of a 25 nm thick bare region of gold films was about 8 min. The same procedure was used to pattern thicker gold films. However, it was not possible to pattern films of 50 nm and 100 nm thickness. Results in literature reveal that alkyl thiol based SAMs can only withstand the ferri/ferrocyanide etch for a limited period of time. Subsequently only thin metal films can be patterned by the ferri/ferrocyanide etchant.

![Fig. 4.3: Micrographs of patterned gold film on a silicon wafer (a) and a plastic foil (b). The gold films were patterned using an ECT SAM as etch resist and wet chemical etching by a ferri/ferrocyanide solution.](image)

The same experiment was repeated for silver films patterned with ECT SAMs. In this case, the thicknesses of the metal film were 30 nm and 300 nm. The films were deposited on glass substrates. Micrographs of the patterned silver films are shown in Fig. 4.4. Structures down to the 1 µm were patterned using this method. The resolution of the patterning process was limited by the resolution of the stamps, which were realized by optical lithography. It can be expected that structures in the submicron range can be patterned if the stamps are fabricated by electron beam lithography. The results indicate that significantly thicker silver films can be patterned by this approach. Up to the knowledge of the authors it was the first time that such thick metal films were patterned by using SAMs as an etch resist. The time required for the complete etching of 300 nm thick silver film was about 2 min. A systematic inspection of the metal structures on the glass substrate showed that the density of defects increases with increasing thickness of the metal film.
In the following the two etching processes for the gold and the silver will be compared in terms of the absolute etching window, the relative etching and the selectivity. The three parameters will be briefly defined in the following:

I) **Absolute etching window**: Period between the complete patterning of the metal and the removal of the SAMs by the etchant;

II) **Relative etching window**: Ratio of the absolute etching window to the etching time needed to remove the metal films plus the SAMs;

III) **Selectivity**: Ratio of the etching rates between the SAMs covered and bare metal surfaces.

The etching window was investigated for the two different metals – silver and gold. In the study, bare and SAMs covered metal film regions were used to obtain quantitative data in both metal types and qualitative comparison between the two metal types in terms of the three parameters mentioned above. The composition of the ferri/ferrocyanide solution etching solution was the same for all set of experiments in both metal types and was prepared according to Ref. 4.10, where it is standard composition. In the study, the time where the first defects over the SAM covered region of the metal film was approximated as the starting time where the SAMs covered region is attacked. This approximation was made because of the difficulty to know the exact starting time where the SAMs covered region starts to be etched. However, there can be little deviation from the exact etching window, the approximated value is used as a comparison of etching window for different film thickness of the two metal types.

The etching time difference for SAMs covered and bare region of the metals is one fundamental parameter in the study. A prolonged time of etching after the complete etching of the bare region (without having a defect on the SAMs region) were made for samples of silver films and the time where the first defects on SAMs region were recorded. A maximum etching window (~ 50 sec) of the silver film was observed for the lowest film (30 nm) thickness. A reduction of the etching window was also observed as the metal film thickness increase. Here, it is important to note that the removal of the
metal film over the substrate was tested by conductivity measurement. In the study, it has been observed that, a further stay of etching above a critical time limit attacks the SAM covered region of the metal. In other words, the etching solution becomes non-selective after a critical time. As an example, based on the results, a 100 nm SAM covered silver film was etched after 10 min. Based on general etching trend, it is also expected that the time required for removing the SAMs covered region of the metal will increase with film thickness.

A similar study was done on 17 nm and 25 nm thick gold films. The approximated etching window for 25 nm gold film thickness was ~ 5 min. As compared to 17 nm gold films, the etching window of 25 nm gold was lowered with a few orders of magnitude. It has been also observed that a further stay of etching above ~ 25 min. removes all the metal films on either the bare or SAM covered region of gold with a film thickness of 17 nm. Again, the time required for complete etching of the SAMs covered or bare gold will increase with film thickness.

Based on the results, comparisons of the three parameters that are mentioned above were made on gold vs. silver. First, it was clearly observed that the etching rate of gold was very low as compared to that of the etching rate of silver. Second, a comparison of gold and silver of the same film thickness shows that the relative etching window of silver is larger than gold. These differences in etching rate and etching window in gold and silver can be due to the difference in the chemistry of the material, which affects the rate of chemical reaction of the etching process. Fig. 4.5 shows the ideal etching trend of silver and gold using the ferri/ferrocyanide. As shown in Fig. 4.5a the surface has two regions, i.e., regions covered with the thiol SAMs and the bare region. While etching with the solution, we have observed that the etching window (∆, as seen on Fig. 4.5b) is different for different film thickness and different materials. Besides, the time required for etching the bare region increases with film thickness. As a result, the etching window of the same material increases with reduction of film thickness as shown in Fig. 4.5b.

Furthermore, it is clear that the SAM has only surface property or has no bulk property and thus the time for the metal film to withstand the etching solution is independent of the metal film thickness. Thus, as can be seen on Fig. 4.5, the SAMs covered metal film thickness starts to decrease after a fixed time for different metal film thickness. However, it is important to note that the total time required for complete etching of different film thickness of the same metal type increases with the metal film thickness. On the other hand, it was observed that the time required for removal of SAMs over gold is higher than the time required for removal of SAMs over silver. These important and interesting phenomena can be due to the difference in interfacial chemistry of the SAM vs. metal film. In other words, the radical group is the protective layer and removing the radical layer from the metal film depends on bonding between the head group of the SAM and the metal surface atoms. Thus, this difference may indirectly show us that the sulphur-gold bond is more resistant to the etching solution than the sulphur-silver bond. The schematics in Fig. 4.5 represent all these phenomena explained above. It correlates the general fundamental etching trend of gold and silver using a SAM as etch resist and a ferri/ferrocyanide etching solution process. The study has a practical implication in controlled etch processing of the two metals when thiol SAMs are used as an etch resist.
In addition to the study in terms of etching window and etching rate, the use of SAMs as etch resist is used to realize source drain contacts of an organic TFT over oxidized silicon substrate. Furthermore, the method is also used to pattern coils over flexible plastic foil. Fig. 4.4 presents patterned gold electrodes over rigid silicon (a) and flexible foil (b). The method has realized submicron resolution structures. Such patterned
structures can be used for the realization of electrodes organic TFTs [4.11]. However, here, it is important to note such long radical chain of the SAMs resist, which stays over the metal film, can have an effect on the contact resistance of the TFT [4.12]. Thus, there is a need to remove the long chained radical SAMs and substitute it with the preferred thiol SAMs that are relatively short and have phenol group. The preferred thiol based SMAs that can be used to improve the performance of the OTFT are discussed in chapter 8. Again the formation of this phenol based needs hydrophilic surface. Such removal of SAMs cannot be done by chemical treatment. To address this problem, the samples treated with ECT SAMs were exposed to UV light. After the UV exposure, the sample is ready for phenol based thiol surface treatment and fabrication of organic TFT.

4.4 Alkyl thiol self-assembled monolayers as dewetting agent

Using a printed thiol based SAMs as an etch resist seems to be an ideal method to pattern metallic microstructures. However, the use of a ferri/ferrocyanide solution is rather hazardous. The ferri/ferrocyanide solution does not comply with standard chemicals used in semiconductor processing. In order to avoid using a hazardous etching solution a new patterning method was developed. In this case the thiol self-assembled monolayer is used as a selective wetting agent rather than a etch resist or etch mask. In the first step the thiol SAM is microcontact printed on the metal surface. The area covered with the thiol SAMs turns hydrophobic, whereas the uncovered areas stay hydrophilic. Such patterned surface modification allows for selective wetting of polymers or resists over the hydrophilic surfaces.

A detailed description of the selective wetting of polymers or resists on functionalized surfaces is described in chapter 3. Therefore, the physics of selective dewetting of polymers on functionalised surfaces will not be discussed here for the second time. Instead, here emphasis is given to the state of the art and application selective dewetting of resist/polymer over gold surface. In this study, polymethylmethacrylate (PMMA) was used to selectively wet the gold surface. Subsequently, the patterned polymers were used as etch mask to pattern the gold film by potassium iodide/iodine (KI/I$_2$) etching solution (3:10 of KI/I$_2$: H$_2$O etching solution). The KI/I$_2$ solution etches the gold together with the SAMs. Thus, the SAM does not have to be removed by an UV treatment.

A micrograph of gold stripes patterned by a diluted solution of KI/I$_2$ is shown in Fig. 4.6. Structures down to 1 $\mu$m were patterned by this approach. The gold film has a thickness of 20 nm. A titanium layer was used as adhesion layer for the gold film. The titanium film was removed by a sulphuric acid solution, after patterning the gold film. Since the KI/I$_2$ solution does not attack the resist pattern on the surface thick or even very thick metal films can be patterned by this approach.

The same patterning procedure was also applied to pattern gold structures on a flexible plastic foil. Patterned gold structures on a 2 cm by 2 cm large polyethylene terephthalate (PET) plastic foil are shown in Fig. 4.7. Thus, the method has witnessed its applicability in flexible electronics with a relatively environmental friendly etchant.
4.3 Summary

In summary, thiol based SAMs can be used as etch masks to pattern thin metallic films like gold, silver or copper. In this study, silver and gold films were patterned over flexible and rigid substrates using alkyl thiol SAMs as etch resist and ferri/ferrocyanide as etchant. The patterning process was systematically investigated in terms of the available etching window and the etching selectivity. A comparison of the patterning process for gold and silver shows that the selectivity is higher for silver resulting in a larger relative etching window. Silver films with a thickness of up to 300nm were patterned by this approach. Generally, the use of thiol SAMs as an etch resist in combination with a ferri/ferrocyanide solution is a suitable method to pattern thin metal films over a large area. Nevertheless, the integration of the process in a standard semiconductor process flow is limited, since the ferri/ferrocyanide etching solution is not compatible with standard processes. In this study, a new method was developed, which combines \( \mu \text{CP} \) of thiol SAMs with selective surface dewetting/wetting. The printed regions are hydrophobic, while the unprinted regions stay hydrophilic. The hydrophilic/hydrophobic patterns were used to selectively deposit polymers and resists on the substrates. Subsequently, the patterned polymer is used as etch resist and the gold and silver films were patterned by a KI/I\(_2\) etching solution. The patterning method is relatively
environmental friendly method as compared to the method using a ferri/ferrocyanide etchant. The method is also allows for patterning of thick metal films, which not possible using the thiol SAMs as etch resist.

References

5 Organic Thin Film Transistors

5.1 Introduction

Research on organic electronics has been initiated by the prospect of low cost, flexible, thin, and lightweight electronics. Organic materials are well suited for large area and low temperature processing. Research is carried out on organic light emitting diodes (OLEDs) for lighting and display applications, organic solar cells and organic thin film transistors (OTFTs). Organic thin film transistors (TFTs) are potential building blocks for organic displays, integrated circuits like radio frequency identification (RFID) tags, smart cards and the like. Progress in organic electronic has been mainly sustained by improvements of the material properties [5.1,5.2] and the processing techniques [5.3,5.4].

An organic thin film transistor (OTFT) is a device that uses organic semiconductors like conjugated polymers or small molecules as an active layer to switch or control a current flow between the drain and source electrode of the transistor. The concentration of charges in the channel of the transistor is controlled by applying a voltage to the source and the gate electrode of the transistor. The schematic cross section of an OTFT is shown in Fig. 5.1. The drain current of the transistor is determined by the electronic properties of the organic channel material, the applied voltages and the device geometry. The device geometry of the OTFTs is represented by the channel length (L), channel width (W), dielectric constant (\( \varepsilon \)) and thickness (d) of the dielectric. In the case of all-organic TFTs the dielectric and the electrodes are realized by insulating and conducting polymers.

![Schematic cross section of an organic thin film transistor](image)

*Fig. 5.1: Schematic cross section of an organic thin film transistor. L and W represent the channel length and width of the transistor.*

In this chapter the basics of organic thin film transistors will be introduced. The most commonly used organic semiconductors will be introduced in section 5.2. In section 5.3, the different device structure of thin film transistors (TFTs) will be introduced. The device fabrication of the organic semiconductors is introduced in section 5.4. The charge transport of organic semiconductors is compared to inorganic semiconductors in section
5.5. The basic operation principle of organic TFTs is presented in section 5.6. The electrical characteristics of organic TFT will also be presented including the parameter extraction of is described in section 5.7. Finally, a summary of the chapter is given in section 5.8.

5.2 Organic semiconducting materials

Organic materials are mainly composed of hydrogen and carbon. The vast majority of organic materials are insulators. However, certain polymers exhibit semiconducting or conducting properties. Of the organic materials, only conjugated (alternating single and double bond) materials can be considered as semiconductor material. These organic semiconductor materials are generally distributed in two classes: small molecules ("short" chain materials) and polymers (long chain materials). Organic semiconductors mainly consist of a chain of benzene and/or thiophene (four carbon atoms and one sulfur atom in a five-membered ring) rings. Fig. 5.2 shows some of the organic semiconductors in the two major classes.

Fig. 5.2: Typical organic semiconductors used as active materials in organic thin film transistors: small molecules (a) and polymers (b).

Polymeric semiconductors are molecular chains formed by repeated units called monomers. In contrast to insulating polymers, the semiconducting polymers contain
conjugated bonds resulting in semiconducting or conducting properties. These materials mainly contain benzene molecules (e.g., Poly(9,9-dioctylfluorene-co-bithiophene), F8T2) or thiophenes (e.g., poly(3-hexylthiophene, P3HT) molecules (see Fig. 5.2). Semiconducting polymers are mainly deposited by solution methods.

The class of small molecules consists of acenes, oligothiophenes and other small molecules such as perylene and pathalocyanaine. The small molecules are composed of either benzene molecules or combinations of benzene and thiophene molecules (Fig. 5.2a). Other small molecules are called oligothiophenes. Oligothiophenes are composed of chains \((n < 10)\) of thiophenes that are substituted, or non-substituted by linear alkyl \((C_nH_{2n+2})\) groups at its end.

Of the many types of small molecules, pentacene (see Fig. 5.2a) is the most commonly applied material in organic thin film transistors [5.4, 5.5]. The material consists of five linearly arranged benzene rings and belongs to the class of polyacenes. The material is known for its high structural order. As a result the material exhibits one of the highest charge carrier mobilities of organic materials.

### 5.3 Processing semiconductors

Several methods are used to deposit organic materials. The main deposition methods can be categorized in solution and evaporation methods.

Solution processing is an ideal method to deposit soluble polymers over large areas. Soluble polymers can be processed by spin coating, dip coating, aerosol spray, doctor blading, inkjet printing and the like.

Evaporation methods, also called physical vapour deposition (PVD), are used for the deposition of small molecules. The PVD is further classified into two organic molecular beam deposition (OMBD) and organic vapour phase deposition (OVPD). In the OMBD process an organic material is heated under high vacuum \((10^{-6}-10^{-12} \text{ Torr})\) and directly evaporated onto a substrate. Monolayer growth of organic thin films with extremely high chemical purity and structural precision is possible with this deposition method [5.6]. On the other hand, OVPD is a process in which a carrier gas like nitrogen or argon is used to transfer the organic molecules from the evaporation source to the substrate.

### 5.4 Thin film transistor structures

Thin film transistors consist of a gate electrode, an insulating layer, an organic semiconductor, and source/drain electrodes. Typically, these TFT components are fabricated over a neutral substrate like glass or a flexible plastic foil. In terms of the device structure different transistor geometries can be distinguished. Depending on the arrangement of the gate and the drain/source electrodes four different types of thin film transistors can be realized. All four-device structures are shown in Fig. 5.3. The selection of the different device structures depends on several factors including the processing conditions and the available materials. For example, amorphous silicon TFTs are typically realized in bottom gate configuration, whereas polysilicon TFTs are usually realized in top gate configuration. Polymer TFTs can be realized in top or bottom gate thin film transistors. The appropriate device structure mainly depends on the
applied gate dielectric. Small molecule thin film transistors are usually realized in bottom gate configuration.

![Device geometries of thin film transistors](image)

**Fig. 5.3:** Device geometries of thin film transistors: (a) top-gate coplanar TFT; (b) top-gate staggered TFT; (c) bottom-gate inverse staggered TFT; and (d) bottom-gate inverse coplanar TFT

### 5.5 Charge transport in organic semiconductors

The main difference between organic and inorganic semiconductor originates from the charge transport mechanisms. This mechanism is in turn dependent on the type of interactions between the building blocks and the degree of order of the atoms or molecules. In inorganic crystalline semiconductors like silicon the atoms are bonded by strong covalent bonds, and the charge transport takes place in a well-defined electronic band. However, in organic semiconductors the molecules are weakly held by van der Walls interactions, and are relatively poorly ordered. Besides, charge carriers cannot move easily through the material due to large intermolecular distances and small intermolecular orbital overlap as compared to crystalline semiconductors. As a result, organic semiconductor exhibit lower carrier mobility as compared to their counterparts - inorganic semiconductors.

Organic semiconductors are based on orbital configurations of carbon atoms, which are referred to as \(sp^2\)-hybridizations and \(p_z\)-orbitals. Of the four outer electrons, the \(sp^2\)-orbitals lie on a plane as shown on Fig. 5.4a. The \(p_z\)-orbitals are in the plane perpendicular to the plane \(sp^2\)-orbitals.
Fig. 5.4: Configuration of the six \( sp_2 \) and two \( p_Z \) orbitals of ethane (a) their respective energy levels (b).

An orbital overlap of two \( sp_2 \)-orbitals between two carbons form a strong tie called a \( \sigma \)-bond, and the energy difference between the occupied binding orbital (\( \sigma \)) and the unoccupied anti-binding orbital (\( \sigma^* \)) of the \( sp_2 \)-orbitals is quite large, and leads to insulating properties. However, the \( p_Z \)-orbitals form additional \( \pi \)-bonds with bean-shaped probability areas above and below the plane of the atoms (see Fig. 5.4a). This pair of bean-shaped probability areas constitutes one \( \pi \)-bond and the pair of electrons in this bond can be found in either bean-shaped area in the case of bonding, or can be found in different direction (up and dawn) in the case of anti bonding (\( \pi^* \)) (see Fig. 5.4b). The \( \pi \)-bond is relatively weak and the electrons are delocalized. These bonds have much smaller energy differences between the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). Such materials, with alternating \( \pi \)-bonds, exhibit a semiconductor property.

Fig. 5.5: Configuration of \( p_Z \) orbitals at different energy levels and the dependence of the HOMO-LUMO energy gap on the number of \( p_Z \) orbitals. \( N \) represents the number of \( P_z \) orbitals.

When carbon atoms form larger molecules, e.g., pentacene consisting of five benzene rings as the basic unit, there are several \( p_Z \) orbitals, and as a result the width of HOMO and LUMO increases, there by creating a reduced gap (i.e., between the HOMO and
LUMO) as compared to that of ethane (Fig. 5.4). In other words, as the number $p_z$ orbital (NP$_z$) increases (e.g., antracene, tetracene, and pentacene in increasing order of $p_z$ orbitals), the energy gap decreases and the width of the HOMO and LUMO decrease as shown in Fig. 5.5. Consequently, the ordering of such molecules with reduced gap can induce a remarkable charge transport across the molecules and can be used as semiconductor layer in TFT, i.e. the organic semiconductor as an active channel region of a transistor.

5.6 Operation and characterization of organic thin film transistors

An analytical expression of the electrical characteristic of a thin film transistor can be derived by considering the gradual channel approximation. It is assumed the electric field created by the gate voltage, $V_G$, is much larger than the electric field created by the gate voltage, $V_D$. If the gate voltage is higher than the threshold voltage, $V_T$, charges are accumulated in the channel and the transistor turns on [5.7].

![Schematics of a typical organic thin film transistor](image)

*Fig. 5.6: A schematics of a typical organic thin film transistor. The channel length of the transistor is given by $L$.*

The carrier density per unit area in the channel depends on the potential distribution along the channel, $V(x)$ (see Fig. 5.6). The drain current can be written in terms of [5.8]:

$$I_D = \mu \cdot W \cdot Q \cdot F_x,$$

(5.1)

where $W$ is the channel width, $\mu$ is the charge carrier mobility and $F_x$ is the electric field along the channel in the x-direction (Fig. 5.6). By substituting $F_x = -dV(x)/dx$ and $Q = C_G \cdot (V_G - V_T - V)$ Eq. (5.1) can be rewritten as

$$I_D \cdot dx = \mu \cdot C_G \cdot W \cdot (V_G - V_T - V) \cdot dV$$

(5.2)

where $C_G$ is the gate capacitance per area, $\mu$ is the charge carrier mobility, and $W$, $L$ are channel width and channel length of the TFT. By integrating of the current from $x = 0$ to $L$ and integrating of the voltage from $V = 0$ to $V_D$, the drain current of the transistor, $I_D$, can be rewritten in the following form:
The equation is valid for \( |V_D| \ll |V_G - V_T| \). This regime is called linear regime since the drain current is linearly proportional to the drain voltage. This linear relationship can be easily seen from the output (\( I_D \) versus \( V_D \)) characteristics of the device (see Fig. 5.7a).

\[
I_D = \frac{W}{L} \cdot C_G \cdot \mu \cdot V_D \left( V_G - V_T - \frac{V_D}{2} \right), \tag{5.3}
\]

At higher drain voltage, \( |V_D| \geq |V_G - V_T| \), the drain current will start to saturate (see Fig. 5.7a). In this regime, a depletion area forms at the drain current and the channel is pinched off. At this onset, \( V_D = V_G - V_T \). Beyond this value, the regime is called saturation regime. As the current saturates after the pinch-off, the saturation current can be obtained by substituting \( V_D \) by \( V_G - V_T \) to Eq. (5.3) Thus, the drain current in this regime is given by:

\[
I_D = \frac{W}{2 \cdot L} \cdot C_G \cdot \mu \cdot (V_G - V_T)^2. \tag{5.4}
\]

In this regime, the drain current is independent of the drain voltage, but it varies quadratically with the gate voltage in the saturation regime. The drain current at \( V_G = V_T \) is zero and it is referred to as cut-off.

The most important device parameters of a transistor are the charge carrier mobility, the threshold voltage, the sub-threshold slope and the on/off ratio. Ideally the transistors
should exhibit a high charge carrier mobility, high on/off ratio, and low sub-threshold slope and a near zero threshold voltage. All these parameters can be extracted from the transfer curves of a transistor (Fig. 5.7b).

The first and most important device parameter is the charge carrier mobility. The charge carrier mobility is defined as the average charge carrier drift velocity per unit electric field. In other words, the mobility ($\mu$) describes how easily charge carriers can move within the active layer under the influence of an electric field. The charge carrier mobility can be extracted from the transfer characteristic of a transistor in the linear and the saturation regime. The charge carrier mobility in the linear region can be obtained from Eq. (5.4) and is determined by

$$\mu_{\text{lin}} = \frac{L}{W} \cdot \frac{1}{C_G} \cdot \frac{1}{V_D} \cdot \frac{\partial I_D}{\partial V_G}.$$  \hspace{1cm} (5.5)

Similarly, the mobility in the saturation can be obtained from Eq. (5.4) and is extracted in the following way:

$$\mu_{\text{sat}} = \frac{2 \cdot L}{W} \cdot \frac{1}{C_G} \cdot \left( \frac{\partial (\sqrt{I_D})}{\partial V_G} \right)^2.$$  \hspace{1cm} (5.6)

The second important device parameter is the threshold voltage, $V_T$. The threshold voltage can be determined from the linear transfer curve by drawing a linear fit to the drain current in the linear region and extracting the gate voltage at the intersection with the gate voltage axis. The threshold voltage in the saturation region is extracted by linear extrapolating the square root of the drain current. The intersection of the transfer curve with the voltage axis corresponds to the threshold voltage.

Another important device parameter is the sub-threshold slope. A TFT does not turn on abruptly at the threshold voltage $V_T$, instead, there is a region where the drain current increases exponentially with gate voltage. This regime is called sub-threshold regime and described by the subthreshold slope. The subthreshold slope indicates how “fast” the transistor turns on. A small subthreshold slope indicates a “fast” transition from the off- to on- state of the transistor. The subthreshold slope is defined as:

$$S = \frac{\partial V_G}{\partial \log(I_D)}.$$  \hspace{1cm} (5.10)

The fourth important device parameter is the current on/off ratio, which is also called current modulation. The on/off ratio is defined to be the ratio of the drain current in the on- state to the off- state of the transistor. This parameter is a vital requirement for different applications like memory and display application, where a high on/off ratio is more important than a high mobility [5.8]. The $I_{\text{on}}/I_{\text{off}}$ ratio of OTFTs is usually greater than $10^6$, and device and material parameters like film thickness and conductivity of the affects the on/off ratio.

### 5.7 Summary

The performance of organic TFTs has been significantly improved during the last decades. The progress has been caused by distinct improvements of material
processing and device fabrication. Organic semiconductor materials can be classified in small molecules and polymers. Polymers are primarily deposited by solution methods, whereas small molecules are thermally evaporated.

The device design and fabrication of organic TFT has been briefly introduced. Furthermore, the current/voltage characteristic of thin film transistors were introduced, and concepts how to extract the most important device parameters were described.

References

6 Organic Transistors with Printed Electrodes

6.1 Introduction

Organic electronics has attracted much attention in recent years. The prospect of flexible, unbreakable, extremely low-weight electronics at relatively low cost has stimulated a lot of research and development efforts on organic thin film transistors (OTFTs) [6.1-6.3], flexible displays media [6.4], and organic sensor arrays [6.5,6.6]. Such electronic devices can only be realized at low cost if novel material systems and new ways of fabricating the devices and systems are developed. Printing techniques are considered as one of the preferred fabrication methods of large area electronics. Printing techniques allow for the low cost patterning of micro or nano structures over large areas and/or flexible substrate. In this chapter micro contact printing will be used to pattern electrodes of organic thin film transistors. The influence of two different microcontact printing based fabrication methods on the performance of pentacene TFTs will be investigated. The investigations are based on the micro contact printing methods described in chapter 3 and 4. Printed silane or thiol based self-assembled monolayers (SAM) will be used to selective patterning of resists on silicon oxide or gold surfaces. The resist structures allow for the patterning of metallic micro- and nanostructures over large areas by a lift-off or wet etching process, respectively.

The fabrication of the electrodes will be described in detail in section 6.2. The electrical properties of the pentacene thin film transistors will be presented in section 6.3. The transistor with printed electrodes will be compared to pentacene transistors with drain and source electrodes patterned by optical lithography. In particular the influence of contact effects on the transport characteristic and the charge carrier mobility of the organic transistors will be discussed. A simple model will be presented which allows for determining the contact resistance of organic transistors. The two microcontact printing based patterning approaches will be compared in terms of its applicability in organic electronics (section 6.4). Finally the results will be summarized in section 6.5.

6.2 Device fabrication

The schematic cross-section of a pentacene thin film transistors with bottom drain / source electrodes is shown in Fig. 6.1. The bottom drain / source electrodes of the organic thin film transistors were realized by a combination of microcontact printing with a lift-off or a wet chemical etching process. Furthermore, optical lithography was used to realize drain / source electrodes. The samples with drain and source electrodes prepared by optical lithography are used as reference samples. The drain / source electrodes were realized on oxidized silicon wafers. The different fabrication methods used to realize the drain and source electrodes will be briefly described.

Thiol self-assembled monolayers as etch resist:

Patterning of surfaces by thiol SAMs like eicosanethiol (ECT) as etch resist has been demonstrated for gold, silver, copper and palladium. A more detailed description of the patterning process is given in chapter 4. In the following the patterning process is used
to realize gold drain/source electrodes of pentacene thin film transistors. The patterning process is illustrated in Fig. 6.2a. Even though the method allows for the patterning of small structures down to the submicrometer range, the etchant (ferri/ferrocyanide) is not compatible with standard processes in semiconductor electronics. In order to replace the etchant (ferri/ferrocyanide) a new method was developed, in which the noble metal film is patterned by a classical wet etchant.

![Diagram of molecular structure and schematic cross section of a pentacene thin film transistor](image)

*Fig. 6.1: Molecular structure of pentacene (a) and schematic cross section of a pentacene thin film transistor (b). The source and drain electrodes were patterned by microcontact printing in combination with a lift-off process, wet chemical etching, or photolithography.*

**Thiol self-assembled monolayers as surface wetting agent:**

A schematics process flow of the patterning scheme is shown in Fig. 6.2b. The printed eicosanethiol (ECT) SAM is used to functionalize the gold surface. The ECT covered regions turn hydrophobic, while the unexposed or bare regions stay hydrophilic. Subsequently, the sample was dip coated or spin coated by polymethylmethacrylate (PMMA). The resist selectively wets the hydrophilic regions of the substrate, while the hydrophobic regions stay uncoated. Finally, the patterned polymers were used as etch mask to pattern the gold film by potassium iodide/iodine (KI/I₂) etching solution (3:10 of KI/I₂: H₂O etching solution). Using thiol self-assembled monolayers allows for patterning of gold or silver films on rigid or flexible substrates. However, thiol SAMs can only be applied to pattern gold, silver or cooper films. Other commonly used metals like chromium, aluminium or tungsten cannot be patterned by this approach. In order to pattern metals like chromium, tungsten or aluminium a printing based lift-off process was developed, which allows for patterning a variety of conducting and semiconducting materials.

**Silane self-assembled monolayers as surface wetting agent:**

The silane based printing approach facilitates a universal route in patterning a variety of materials on substrates like glass or oxidized silicon wafers. A schematics process flow of the patterning scheme is shown in Fig. 6.3a. The method is comparable to standard photolithography. After forming a resist pattern the metal film is patterned by a lift-off process. The silane SAMs are used to selectively control the wetting properties of
oxidized silicon or glass substrate. Once a resist like polymethylmethacrylate, PMMA, is selectively deposited by dip coated or spin coated over the substrate, the OTS SAMs were removed by a ultraviolet (UV) light exposure. In this experimental octadecyl-trichlorosilane (OTS) was used. Finally, the resist pattern was used to lift-off different metal films like chromium and gold. A detailed description of the patterning process is given in chapter 3.

Fig. 6.2: Patterning of a gold film by a combination of microcontact printing and wet chemical etching: a) Eicosanethiol self-assembled monolayers were printed onto the gold films. The thiol SAM acts a etch mask. The uncoated regions were patterned by a ferri/ferrocyanide etching solution; b) Eicosanethiol self-assembled monolayers were printed onto the gold film to form hydrophilic and hydrophobic regions. The thiol self-assembled monolayers allows for selective wetting of the gold surface by a resist. After patterning the resist film, the gold film can be patterned by a subsequent wet etching step using a potassium iodide/iodine solution (KI/I₂) etching solution.

Optical lithograph:

The schematics process flow of a standard lift-off process is shown in Fig. 6.3b. The resist patterns were realized by conventional optical lithography. The samples with drain and source electrodes prepared by optical lithography are used as reference samples.
Fig. 6.3: Patterning of metal electrodes by a lift-off process using: a) microcontact printing of OTS self-assembled monolayers (SAMs) and selective wetting and; b) photolithography. The resist structures used in (a) is PMMA and the UV light is used to remove the OTS layer from the substrate.

The drain/source electrodes were realized on highly doped silicon wafers. The gate dielectric of the transistor was formed by a 100 nm thick thermal oxide layer. The fabrication process of the pentacene thin film transistors was completed by depositing the pentacene film in an Organic Molecular Beam Deposition (OMBD) system. A further description of the deposition conditions is given in Ref. 6.13. Before depositing the organic semiconductor the oxide surface and the gold electrodes were treated by hexamethyldisilazane (HMDS) and 2-Mercapto-5-nitrobenzimidazole (MNB) SAMs, respectively. Treating the silicon dielectric by HMDS leads to an increase of the effective charge carrier mobility of the transistors by a factor of 2-3 [6.7]. Treating the gold electrodes by MNB leads to an improved charge injection, so that the drain and source contact resistance is reduced by 20%-50% [6.8]. Organic TFTs with a channel length of 20 μm to 140 μm, and a channel width of 4000 μm were realized.

6.3 Characterization of transistors with printed electrodes

After fabricating the devices, OTFTs, the electrical characteristics were measured in the dark at room temperature. The transfer curves of the pentacene thin film transistor with
The drain / source electrodes of the transistor in Fig. 6.4 were patterned by microcontact printing and wet chemical etching (potassium iodide/iodine etching), whereas the drain / source contacts of the transistor in Fig. 6.5 were patterned by micro contact printing in combination with a lift-off process. The transistors exhibit device charge carrier mobilities ranging from of 0.2-0.4 cm²/Vs. The on/off ratio, defined as the ratio of the drain-source current in the on-state and the off-state, were measured to be larger than 7 orders of magnitude. The determined threshold voltages are in the range from -1 V to -3V. The drain current of the thin film transistor in the linear region is described by

\[ I_D = \frac{W}{L} C_G \cdot \mu_{\text{dev}} \cdot V_D \cdot \left( V_G - V_T - \frac{V_D}{2} \right) \], \hspace{1cm} (6.1)

where \( W \) and \( L \) are the width and the length of the channel. \( C_G \) is the gate capacitance per unit area, and \( V_G \), \( V_D \) and \( V_T \) are the gate, drain and threshold voltages, respectively. \( \mu_{\text{dev}} \) is the device charge carrier mobility. The transistor operates in the linear region if \( V_D < V_G - V_T \). Based on Eq. (6.1) the device charge carrier mobility of the transistors in the linear region can be determined by

\[ \mu_{\text{dev}} = \frac{1}{V_D C_G} \cdot \frac{L}{W} \frac{\partial I_D}{\partial V_G} \]. \hspace{1cm} (6.2)
The device charge carrier mobility of the transistors as a function of the gate voltage is shown in Fig. 6.6. The device charge carrier mobility is plotted for a pentacene TFT with drain/source electrodes patterned by microcontact printing in combination with a lift-off process and wet etching. Furthermore, a transistor with electrodes patterned by optical lithography is shown in the Fig. 6.6.

![Device charge carrier mobility graph](image_url)

**Fig. 6.6:** Device charge carrier mobility in the linear regime ($V_D=1$ V) of operation for pentacene transistors with drain and source electrodes prepared by microcontact printing and optical lithography.

The TFTs fabricated by microcontact printing in combination with a lift-off process show a maximum device charge carrier mobility of 0.2 cm$^2$/Vs for a gate voltage of $–3.5$ V. A further decrease of gate voltage beyond $–3.5$V results in a drop of the device charge carrier mobility by 80%. The device charge carrier mobility of the transistor with electrodes prepared by standard photolithography is 2-3 times higher than the device charge carrier mobility of the transistors with electrodes prepared by microcontact printing in combination with a lift-off process. The transistor with drain/source electrodes patterned by microcontact printing in combination wet etching (potassium iodide/iodine etching) exhibits a device charge carrier mobility comparable to transistors with drain/source electrodes patterned by optical lithography. However, the device charge carrier mobility of the transistor with printed and etched drain and source electrodes drops with decreasing gate voltage by 45%, while the device charge carrier mobility for the TFT with drain and source electrodes prepared by optical lithography is only reduced by 25% - 35%.
If the transistors would behave like an ideal transistor described by equation (Eq. 6.2) the extracted charge carrier mobility should be independent of the gate voltage and the device geometry. However, all transistors exhibit a drop of the charge carrier mobility with decreasing gate voltage. The drop of the device charge carrier mobility of the transistor with electrodes patterned by microcontact printed in combination with a lift-off process are distinctly more pronounced than the drop for the transistor with electrodes defined by optical lithography or wet chemical etching.

The drop of the device charge carrier mobility can be caused by trapping in the pentacene film [6.9, 6.10], scattering of charges at the semiconductor dielectric interface or the influence of contacts effects on the device performance [6.11, 6.12]. As pentacene TFTs fabricated on different dielectrics exhibit the same behaviour scattering processes at the dielectric play a minor role in describing the electronic transport of polycrystalline pentacene thin film transistors.

Measurements of transistors with different channel lengths reveal that the extracted device charge carrier mobility strongly depends on the channel length [6.11, 6.12]. The device charge carrier mobility is significantly reduced for transistors with short channel lengths. The experimental results reveal that the drain / source contacts have a distinct influence on the device performance. Therefore, it can be expected that the drop of the device charge carrier mobility as function of the gate voltage in Fig. 6.6 is caused by the influence of drain / source contact effects. However, it is important to note that the influence of the drain and source contacts depends on the method used to realize the drain and source contacts.

In the following the influence of the drain and source contacts on the charge carrier mobility of the OTFTs is investigated. It is assumed that the contact effects can be described by an ohmic contact resistance. Even though the contact behaviour might be non-ohmic, a certain degree of inaccuracy might be accepted since the assumption of an ohmic contact behaviour allows for providing an analytical relationship between the charge carrier mobility and the contact effects. The drain and source contact resistances cause a voltage drop at the contacts with increasing drain current. It is assumed that the transistor can be described by a drain resistance, $R_D$, a source resistance, $R_S$, and the channel resistance, connected in series. The sum of the drain resistance, $R_D$, and source resistance, $R_S$, is defined as the drain / source contact resistance, $R_C$. The electrical equivalent circuit for a transistor with ohmic contacts is given in Fig. 6.7.

![Fig. 6.7: Equivalent circuit of a thin-film transistor including ohmic contact resistances.](image)

In order to account for the influence of the contacts on the drain current in the linear region the drain voltage $V_D$ and gate voltage $V_G$, in Eq. (6.1) is replaced by $V_D - I_D R_C$, and $V_G - I_D R_S$, respectively. The term “$V_D - I_D R_C$” represents the actual voltage drop across the channel of the transistor. Here, it is important to note that $R_S$ and $R_D$
correspond to the source and drain resistance, which are expected to be equal. Thus, the drain current can be described by

\[ I_D = \frac{W}{L} C_G \mu_0 \left[ (V_G - I_D R_S) - V_T - \frac{(V_D - I_D R_C)}{2} \right](V_D - I_D R_C), \]  

(6.3)

where \( \mu_0 \) is defined to be the intrinsic charge carrier mobility of the transistor. Rewriting Eq. (6.3) leads to the following expression for the drain current:

\[ I_D = \frac{W}{L} C_G \mu_0 \frac{L}{L + WC_G \mu_0 R_C} \left( V_G - V_T - \frac{V_D}{2} \right) V_D \cdot \left( V_G - V_T - \frac{V_D}{2} \right). \]  

(6.4)

Based on Eq. (6.4) an expression for an effective charge carrier mobility, \( \mu_{\text{eff}} \), of the transistors as a function of the channel length and the contact resistance can be determined [6.23]:

\[ \mu_{\text{eff}} = \mu_0 \frac{L}{L + \mu_0 WC_G R_C} \left( V_G - V_T - \frac{V_D}{2} \right). \]  

(6.5)

In order to derive an expression for the drain current in the saturation region the drain voltage, \( V_D \), in Eq. (6.1) was substituted by \( V_G - V_T \) leading to the following equation:

\[ I_D = \frac{W}{2L} C_G \cdot \mu_{\text{dev}} \cdot (V_G - V_T)^2. \]  

(6.6)

Eq. (6.6) is valid for \( V_D \geq V_G - V_T \). The device charge carrier mobility, \( \mu_{\text{dev}} \), in the saturation region of the transistor can be calculated according to

\[ \mu_{\text{dev}} = \frac{1}{C_G} \cdot \frac{2L}{W} \left( \frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2. \]  

(6.7)

In order to derive an expression for the drain current in the saturation region, which takes the influence of the contact effects into account the drain voltage, \( V_D \), in Eq. (6.4) was substituted by \( V_G - V_T \). Thus, the following expression for the drain current in the saturation region can be derived as:

\[ I_D = \frac{W}{2L} C_G \mu_0 \frac{L}{L + WC_G \mu_0 R_S} (V_G - V_T)^2. \]  

(6.8)

Based on Eq. (6.8), the following expression for the effective charge carrier mobility in the saturation regime can be derived:

\[ \mu_{\text{eff}} = \mu_0 \frac{L}{L + \mu_0 C_G R_S} \left( V_G - V_T \right). \]  

(6.9)

In the following the modified transistor model was used to determine the intrinsic charge carrier mobility, the threshold voltage and the contact resistance of the pentacene thin film transistor with drain / source electrodes patterned by microcontact printing and optical lithography.
Fig. 6.8: Drain current (a) and charge carrier mobility (b) of a pentacene thin film transistor with drain and source electrodes prepared by photolithography. The TFT is measured in the linear regime ($V_D=-1$ V).

A) Pentacene transistors with drain and source electrodes fabricated by photolithography

The transfer curves of a pentacene TFT with drain and source electrodes patterned by photolithography is shown in Fig. 6.8. The measured drain current was fitted using the ideal transistors Eq. (6.1) and the modified transistor Eq. (6.4). Fig. 6.8a exhibits the fits
of the drain current in the linear regime. For gate voltages larger than -3.5 V the transistor operates in the saturation region \((V_G \geq V_D + V_T)\). Since the contact resistance for the transistor with drain and source electrodes patterned by photolithography is small in comparison to the channel resistance the contact resistance has only a small influence on the drain current in the linear region.

A good agreement between the experimental data and the fit was achieved for equation 6.1 and 6.4. Taking the contact resistance into account, an intrinsic charge carrier mobility of \(\mu_0 = 0.39 \text{ cm}^2/\text{Vs}\), a threshold voltage of \(V_T = -2.4 \text{ V}\) and a contact resistance of 0.93 k\(\Omega\cdot\text{cm}\) was determined for a transistor with a channel length of 50 \(\mu\text{m}\). As a comparison the channel resistance, which can be calculated by

\[
R_{\text{on}} = \frac{\partial V_D}{\partial I_D} \approx \frac{L}{W C_m \mu_{\text{dev}} (V_G - V_T)}
\]  

(6.10)

is determined to be equal to 49 k\(\Omega\cdot\text{cm}\). Eq. (6.5) was used to describe the drop of the charge carrier mobility as a function of the gate-source voltage in Fig. 6.8b. The drop of the charge carrier mobility can be described by using the parameters stated in Tab. 6.1. The measured drain current in the saturation regime was also fitted by using the ideal transistor Eq. (6.6) and the modified transistor Eq. (6.8). The intrinsic charge carrier mobility, the threshold voltage and the contact resistance were obtained from the fit of the experimental data. The extracted device parameters are comparable to the parameters obtained in the linear regime. A summary of the different device parameters for the TFT with source drain electrodes patterned by photolithography is given in Tab. 6.1.

<table>
<thead>
<tr>
<th>Extracted device parameters</th>
<th>Charge carrier mobility [cm(^2)/Vs]</th>
<th>Threshold voltage [V]</th>
<th>Contact resistance [k(\Omega\cdot\text{cm})]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>0.4 / 0.42</td>
<td>-1.2 / -1.0</td>
<td>-</td>
</tr>
<tr>
<td>Fit by ideal transistor model</td>
<td>0.35 / 0.36</td>
<td>-2.1 / -0.3</td>
<td>-</td>
</tr>
<tr>
<td>Fit by transistor model including contacts</td>
<td>0.41 / 0.42</td>
<td>-2.4 / -1.1</td>
<td>0.93 / 1.3</td>
</tr>
</tbody>
</table>

Tab. 6.1: Transistor parameters for a pentacene TFTs with drain and source electrodes patterned by photolithography. The parameters are stated for the linear (left) and the saturation (right) regime.
Fig. 6.9: Measured and fitted drain current (a and c) and effective charge carrier mobilities (b and d) of a pentacene thin film transistor with drain/source contacts prepared by microcontact printing and wet chemical etching (potassium iodide/iodine etching) in the linear (a, b) and saturation (c, d) region of operation. The linear and saturation regimes were measured at $V_D=-1 \text{ V}$ and $V_D=-10 \text{ V}$, respectively.
B) Pentacene transistors with drain and source electrodes fabricated by microcontact printing and wet chemical etching

In the following, the influence of contact effects on the device charge carrier mobility will be discussed for TFTs with source / drain electrodes patterned by microcontact printing and wet chemical etching (Fig. 6.2b). The transfer characteristic of a TFT with source / drain electrodes patterned by microcontact printing and wet etching (potassium iodide/iodine etching) is shown in Fig. 6.9. The channel length and width of the TFT was 110 µm and 4000 µm, respectively. The transistor exhibits a device charge carrier mobility of 0.3–0.4 cm²/Vs and a threshold voltage of -2.5 V. Furthermore, the transistor exhibits an on/off ratio of more than 6 orders of magnitude at a gate voltage of ~20V.

The drain current in the linear regime of the TFT was fitted by the ideal transistor equation (Eq. 6.1) and modified transistor model taking the influence of the contacts into account (Eq. 6.4) as shown in Fig. 6.9a. Fitting the experimental data allows for determining the intrinsic charge carrier mobility, the threshold voltage and the contact resistance of the pentacene TFT in the linear regime. Using the ideal transistor equations does not allow for a good fit of the drain current in the linear regime. However, a good agreement between the experimental data and the fit was observed when taking the contacts effects in to account. An intrinsic charge carrier mobility of 0.33 cm²/Vs, a threshold voltage of -3 V and a contact resistance of 2 kΩ·cm were determined when taking the contact effects into account. A summary of the device parameters is given in Tab. 6.2.

<table>
<thead>
<tr>
<th>Extracted device parameters</th>
<th>Charge carrier mobility [cm²/Vs]</th>
<th>Threshold voltage [V]</th>
<th>Contact resistance [kΩ·cm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>0.33 / 0.30</td>
<td>-2.5 / -1.0</td>
<td>-</td>
</tr>
<tr>
<td>Fit by ideal transistor model</td>
<td>0.32 / 0.26</td>
<td>-1.8 / -0.6</td>
<td>-</td>
</tr>
<tr>
<td>Fit by transistor model incl. contacts</td>
<td>0.35 / 0.32</td>
<td>-3.0 / -1.5</td>
<td>2.0 / 3.2</td>
</tr>
</tbody>
</table>

*Tab. 6.2: Transistor parameters for a pentacene TFTs with drain and source electrodes patterned by micro contact printing and wet etching. The parameters are stated for the linear (left) and the saturation (right) regime.*

Furthermore, the charge carrier mobility of the transistor with drain and source contacts prepared by microcontact printing and wet chemical etching was fitted by using Eq. 6.5. Equation 6.5 allows for describing the drop of the charge carrier mobility of the TFT as a function of gate voltage (see Fig. 6.9b). The fit of the transfer curve in the saturation region is shown in Fig. 6.9c. According to Eq. (6.9) an effective charge carrier mobility of 0.32 cm²/Vs, a threshold voltage of -1.5 V, and a contact resistance of 3.2 kΩ·cm were extracted. Again a good agreement between the experimental data and the fit was
achieved if the influence of the contacts was taken into account, i.e., Eq. (6.8). The effective charge carrier mobility in the saturation region as a function of the gate voltage is plotted in Fig. 6.9d. Again a drop of the effective charge carrier mobility is observed with decreasing gate voltages.

The extracted parameters for the effective charge carrier mobility and the contact resistance in the linear and the saturation region are almost identical (Tab. 6.2). Eq. (6.9) is used to describe the drop of effective charge carrier mobility of the TFT as a function of the gate voltage. The drop of the effective charge carrier mobility in the saturation regime is also described by using the parameters in Tab. 6.2.

C) Pentacene transistors with drain and source contact prepared by microcontact printing and lift-off process

In the following, the influence of contact effects on the charge carrier mobility of pentacene TFTs with drain / source electrodes fabricated by microcontact printing and a lift-off process is presented. The transfer characteristics of the TFT fabricated by the process flow described in Fig. 6.3b is shown in Fig. 6.10. The channel length and width of the TFT was 40 \( \mu \text{m} \) and 4000 \( \mu \text{m} \), respectively. The transistor exhibits a device charge carrier mobility of 0.18 - 0.2 cm\(^2/Vs\), a threshold voltage of 0.2 V and an on/off ratio of more than 6 orders of magnitude at a gate voltage of –20V.

In the following, the influence of contacts effect on the performance of TFTs with drain / source electrodes fabricated by microcontact printing and a lift-off method is described. The investigation was carried according to the description in subsection A and subsection B of section 6.3. The intrinsic charge carrier mobility, the threshold voltage and the contact resistance of the pentacene TFT in the linear regime was determined by fitting the transfer curve by Eq. 6.1 and Eq. 6.2 (see Fig. 6.10a). A good agreement between the experimental data and the fit was observed when the influence of the contacts was taken in to account.

<table>
<thead>
<tr>
<th>Extracted device parameters</th>
<th>Charge carrier mobility [cm(^2/Vs)]</th>
<th>Threshold voltage [V]</th>
<th>Contact resistance [k(\Omega\cdot\text{cm})]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>0.2 / 0.18</td>
<td>-1.5 / 0.2</td>
<td>-</td>
</tr>
<tr>
<td>Fit by ideal transistor model</td>
<td>0.17 / 0.12</td>
<td>0.3 / 0.8</td>
<td>-</td>
</tr>
<tr>
<td>Fit by transistor model incl. contacts</td>
<td>0.21 / 0.26</td>
<td>-1.2 / -1.0</td>
<td>13 / 14.2</td>
</tr>
</tbody>
</table>

Tab. 6.3: Extracted device parameters from standard in the linear/saturation regime for pentacene TFTs with drain and source electrodes patterned by microcontact printing and lift-off.
Fig. 6.10: Measured and fitted drain current (a and c) and effective charge carrier mobilities (b and d) of a pentacene thin film transistor with drain/source contacts prepared by microcontact printing and lift-off process in the linear (a, b) and saturation (c, d) region of operation. The linear and saturation regimes were measured at $V_D=-1$ V and $V_D=-10$ V, respectively.
Taking the contact resistance into account an intrinsic charge carrier mobility of 0.21 cm²/Vs, a threshold voltage of -1.2 V and a contact resistance of 13 kΩ·cm was determined for a TFT with the channel length of 40 µm. The fit of the drain current without taking contacts into account distinctly deviates from the experimental data. However, it is important to note that the fit of the drain current with contacts are in line with the experimental values in all three cases. A summary of the determined device parameters is given in Tab. 6.3.

![Atomic force microscope (AFM) image of polycrystalline pentacene films prepared on a silicon dioxide dielectric treated with a hexamethyldisilazane (HMDS) SAM and a gold drain/source electrode treated by 2-Mercapto-5-nitrobenzimidazole (MNB) SAM. The drain/source electrodes were patterned by optical lithography (a) and microcontact printing in combination with a lift-off process (b). Cross-sections of a pentacene thin film transistor with drain/source electrodes patterned by optical lithography (c) and microcontact printing and lift off (d).](image)

**Fig. 6.11:** Atomic force microscope (AFM) image of polycrystalline pentacene films prepared on a silicon dioxide dielectric treated with a hexamethyldisilazane (HMDS) SAM and a gold drain/source electrode treated by 2-Mercapto-5-nitrobenzimidazole (MNB) SAM. The drain/source electrodes were patterned by optical lithography (a) and microcontact printing in combination with a lift-off process (b). Cross-sections of a pentacene thin film transistor with drain/source electrodes patterned by optical lithography (c) and microcontact printing and lift off (d).

In the saturation region, \( V_{DS} \geq V_{GS} - V_T \), the transfer curve of the transistors without the contact effects is described by Eq. (6.6). Taking the contact effects into account, the drain current in the saturation regime is represented by Eq. (6.8). The fit of the transfer curve in the saturation region is shown in Fig. 6.10c. According to Eq. (6.8) an effective charge carrier mobility of 0.26 cm²/Vs, a threshold voltage of -1 V, and a contact resistance of 14.2 kΩ·cm were extracted. The charge carrier mobility in the saturation region as a function of the gate voltage is plotted in Fig. 6.10d. A drop of the effective
charge carrier mobility is observed with decreasing gate voltage in the saturation regime. Based on Eq. (6.6) and Eq. (6.9) a maximum saturation mobility of 0.12 cm²/Vs and 0.2 cm²/Vs and a threshold voltage of 0.8 V / -1 V was determined.

The extracted parameters for the effective charge carrier mobility and the contact resistance in the linear and the saturation region are almost identical (see Tab. 6.3). Eq. (6.9) is used to describe the drop of effective charge carrier mobility of the TFT as a function of gate voltage. The drop of effective charge carrier mobility in the saturation regime is also described using the parameters in Tab. 6.3, which is obtained considering the contacts.

To study the origin of the high contact resistance of the transistors with the printed electrodes atomic force microscope (AFM) measurements of the electrodes were taken. Fig. 6.11 shows atomic force microscope images of pentacene films at the edge between the channel and the contact region. Fig. 6.11a exhibits the image of a pentacene film prepared on a photolithographically patterned drain and source electrode. Fig. 6.11b shows a pentacene film prepared on top of a drain / source electrode patterned by microcontact printing and a lift-off. The thickness of the pentacene film (10-15 nm) and the drain / source electrodes (20 nm) is identical for both samples. The AFM image of a pentacene film prepared on a printing and KI/I₂ etching based patterned drain and source electrode has showed similar morphology and oxide/gold transition coverage like that of the image of the pentacene film prepared on a photolithographically patterned electrodes.

The AFM images in Fig. 6.11 show the typical morphology of polycrystalline pentacene films. The pentacene crystals exhibit a dendritic structure with average crystal diameters of 1 µm in the channel region. The channel region was treated by HMDS prior to the deposition of the pentacene film. The drain / source electrodes were treated by a MNB self-assembled monolayer before bringing down the pentacene molecules. The SAM treatment leads to the formation of a highly ordered pentacene film on top of the gold electrodes. The pentacene crystals exhibit an average diameter of 300 nm. A comparison of the AFM images reveals that the formation of the pentacene film at the edge of the electrode is different for the two samples. A clustering of pentacene molecules can be observed for the sample with printed electrodes (Fig. 6.11b). The clustering might be caused by the formation of a burr-like structure at the edge of the printed electrode. A schematic cross section of the sample is shown in Fig. 6.11c and 6.11d to illustrate the influence of the burr-like structure on the formation of the pentacene film. The selective wetting process leads to the formation of an arc-like resist pattern on the substrate. The arc-like structure prevents a complete lift-off of the deposited metal in the channel region. The high contact resistance of the transistor is caused by the poor injection of holes in the pentacene film due to poor step coverage of the pentacene film at the edge of the transistor. The pentacene film is very thin, so that the pentacene molecules just form a contact with the titanium rather that the gold film.

6.4 Contact effects of printed OTFTs

Pentacene thin film transistors with drain / source electrodes patterned by different microcontact printing methods were compared. Microcontact printing in combination with wet chemical etching or a lift-off process was used to pattern the drain / source electrodes of
the transistors. The electrical performances of the organic transistors were comparable to the electrical performance of OTFTs prepared by optical lithography. Tab. 6.4 summarizes the extracted device parameters of pentacene thin film transistors with drain / source electrodes fabricated by optical lithography, microcontact printing in combination with wet etching and a lift-off process. The electrical performance of the TFTs fabricated by microcontact printing in combination with wet etching is comparable to TFT fabricated by photolithography. However, the charge carrier mobility of TFTs with electrodes fabricated by photolithography and wet etching exceed the effective charge carrier mobility of TFTs with electrodes prepared by microcontact printing and a lift-off process by 40%. The contact resistance of the TFTs with microcontact printed and lifted-off electrodes is 10-14 times than the contact resistance of the TFT with electrodes patterned by photolithography and 5-7 times higher than the contact resistance of the TFT with electrodes patterned by microcontact printing in combination with wet etching.

![Tab. 6.4: Extracted device parameters for pentacene TFTs with drain-source electrodes patterned by photolithograph, and microcontact printing in combination with KI/I₂ wet etching and a lift-off process in the linear/saturation regime.](image)

The TFTs with electrodes prepared by microcontact printing in combination with a lift-off process exhibit an increased contact resistance, which leads to a reduction of the device charge carrier mobility. The contact resistance is increased due to the formation of a burr-like structure at the edge of the electrodes, which limits the injection of charges in the channel of the transistor. The influence of the contacts on the effective charge carrier mobility in the linear and the saturation region was described by a simple model, which accounts for the influence of the drain and source contacts.
The influence of the contacts effects on the device operation of TFTs is not only limited to electrodes prepared by printing approaches. In general, it is well known that the performance of organic transistors is limited by the injection of charges in the channel via metal electrodes [6.2]. Different models have been proposed to describe contact effects in organic thin film transistors ranging from simple ohmic contacts [6.12], to gate-source voltage dependent contact resistances [6.11,6.14-6.17] to anti parallel connected Schottky diodes [6.11]. Recent results show that the contacts between pentacene and noble metals like gold, silver and platinum can be described by Schottky barriers or Schottky diodes [6.18]. However, different barrier heights and different dipole moments were determined by different authors [6.18,6.19]. The barrier height and the dipole moment are influenced by the contact geometry (top versus bottom drain and source contacts), potential SAM treatments of the electrodes and environmental conditions. In particular moisture has a distinguished influence on the injection of charges [6.16]. Therefore, the simple model presented in this chapter provides only an estimate of the contact resistance. The contact resistance is the only free parameter in this model. Other models typically require several fitting parameters. Furthermore, the presented model allows for describing the gate voltage dependent effective charge carrier mobility, which confirms the assumption of an ohmic contact resistance. Nevertheless, further investigations are needed to identify and describe the charge injection in the pentacene films. Scanning probe [6.20,6.21] and four probe measurements [6.22] should provide insights in the charge injection mechanism and the contact behaviour.

6.5 Summary

In summary, the influence of different printing methods on the performance of pentacene TFTs was investigated. Microcontact printing in combination with lift-off process and wet chemical etching was used the fabricated drain and source electrodes of pentacene thin film transistors. The electrical characteristics of TFTs with electrodes patterned by microcontact printing were studied and compared to devices with drain and source electrodes fabricated by photolithography. Pentacene TFTs with drain / source electrodes fabricated by microcontact printing and wet etching exhibited a device charge carrier mobility of up to 0.4 cm²/Vs and on/off ratios of 10⁷. The performance is comparable to TFTs with drain and source electrodes fabricated by photolithography. Transistors with drain and source electrodes fabricated by microcontact printing and a lift-off process exhibit charge carrier mobilities of 0.2 cm²/Vs and on/off ratios of 10⁶. The electrical performance of the organic transistors is distinctly reduced in comparison OTFTs with drain and source electrodes prepared by optical lithography.

A simple transistor model was developed which described the electrical characteristic of the transistors with printed electrodes. The model takes the influence of contact effects on the electrical properties of the transistors into account. The model considers the voltage drop at the drain and source contacts, so that the intrinsic charge carrier mobility and the contact resistance of transistors can be determined. The model reveals that the contact resistance of transistors with drain and source electrodes patterned by a microcontact printing in combination to a lift-off process is increased. Atomic force microscope images indicate that the increased contact resistance is caused by the formation of a burr-like structure at the edge of the contact.
Thus, the combination of microcontact printing with wet etching provides a promising route in preparing pentacene thin film transistors with printed electrodes. The process is compatible with standard processes in large area and microelectronics since environmental friendly chemical are used to pattern the metal electrodes. Therefore, the process can be easily integrated in standard display fabrication process.

References

7 Environmental Stabilities of Pentacene Transistors

7.1 Introduction

The interest in organic electronics can be attributed to the emerging demands in novel display media (active and passive) on low cost and/or flexible substrates. Of organic materials, Pentacene (C_{22}H_{14}) has demonstrated one of the highest charge carrier mobilities [7.1-7.2]. The progress of organic electronics has been caused by distinct improvements of the material and device properties [7.2-7.4]. Hole carrier mobilities exceeding 3.0 cm²/Vs were reported for polycrystalline pentacene TFTs by Kelly et al. [7.2] and Klauk et al. [7.4]. Therefore, pentacene thin film transistors are promising candidates for organic electronics applications. Nevertheless, complex organic electronic systems like radio frequency identification tags or displays can only be realized if the device operation is stable and the transistors can be manufactured reproducibility. However, the electrical stability of organic thin film transistors is affected by environmental conditions like oxygen or moisture [7.5-7.7]. The sensitivity of the device to environmental conditions depends strongly on the structural properties of the pentacene film, and the interfaces between pentacene and the contacts [7.8-7.14].

In order to gain insights in the electronic transport properties of polycrystalline pentacene TFTs and to study the environmental stability of the devices electrical in-situ and ex-situ measurements of pentacene TFTs were carried out. The influence of environmental conditions was studied by exposing the TFTs to dry oxygen and moisture. The fabrication of the device structures is described in section 7.2 of the chapter. The environmental stability of the pentacene TFT will be presented in section 7.3. In section 7.3.1 the influence of dry oxygen on the device behaviour is described, whereas in section 7.3.2, the effect of air and moisture on the transfer characteristic is presented. The influence of impurities on the device operation and the electrical stability of the devices will be discussed in section 7.4, before summarizing the results and the discussion in section 7.5.

7.2 Device fabrication

The cross section of a staggered pentacene thin film transistor with bottom drain and source contacts is shown in Fig. 7.1.

![Fig. 7.1: A schematic cross section of a staggered polycrystalline pentacene thin film transistor.](image-url)
A highly doped silicon wafer was used as a substrate. The gate dielectric of the transistor was formed by a 50 nm thick silicon oxide layer. Bottom drain and source contacts were defined by optical lithography. In order to improve the adhesion of the gold drain and source contacts on the substrate a 2-3 nm thick titanium film was evaporated prior to the gold film. Before bringing down the pentacene molecules the thermal oxide was treated by hexamethyldisilazane (HMDS). The pentacene film was evaporated by an Organic Molecular Beam Deposition (OMBD) system.

![Schematic cross section of an Organic Molecular Beam Deposition system. The system allows for the in-situ electrical characterization of different transistors at the same time.](image)

A schematic cross section of the deposition system is shown in Fig. 7.2. The pentacene molecules were deposited by organic molecular beam deposition using a deposition rate of 0.5 Å/s. The source material was two times sublimation purified before depositing the molecules at a base pressure of $5 \times 10^{-6}$ Pa. The films were prepared by keeping the substrate temperature constant at 70 °C. The source temperature was kept constant at 275 °C while depositing the pentacene films. The final pentacene layer has a thickness of 10 nm. Device structures were fabricated ranging from 2 μm to 50 μm channel length. The deposition system allows for an in-situ electrical characterization of the transistors in vacuum.
7.3 Influence of environmental conditions on device stability

7.3.1 Influence of oxygen on the device performance

Understanding the electronic transport of organic semiconductors is essential to improve the device performance of thin film transistors. The transfer characteristic of a polycrystalline TFT fabricated on thermal oxide and measured in high vacuum is shown in Fig. 7.3. The transistor has a channel length of 20 µm and a width-to-length ratio (W/L ratio) of 10000. The transistor was measured under high vacuum (~10^{-6} Pa) at room temperature. The transistor exhibits a mobility of 0.5 cm²/Vs and an on/off ratio larger than 7 orders of magnitude. The transistor exhibits a subthreshold slope of 0.2 V/decade, which is very low for pentacene TFT prepared on 50 nm of thermal oxide. The charge on the gate, which is required to modulate the drain current by one order of magnitude, is typically 2 times higher assuming the subthreshold slope to be normalized by the gate capacitance [7.12]. The onset of the drain current is observed for very small negative voltages. The onset voltage can be defined as the gate voltage for which the drain current starts to increase.

![Fig. 7.3: Transfer characteristic of a pentacene TFT for drain voltages of -1 V and -10 V. The transistor was prepared and characterized under vacuum (~10^{-6} Pa) conditions.](image)

![Fig. 7.4: In-situ measurements of the transfer characteristic of a pentacene TFT for a drain voltage of -1 V. The transistor was exposed to dry oxygen leading to acceptor-like states, N_A, in the pentacene film.](image)
In the following the sample was exposed to dry oxygen for several minutes (> 30 min.). The concentration of oxygen was controlled by the pressure in the high vacuum chamber. Due to oxygen exposure the onset of the drain current shifted towards positive gate voltages. The charge carrier mobility and the threshold voltage of the transistors were not affected by the oxygen contamination. Measurements of the device characteristic were carried out until no further change of the transfer characteristics was observed. The transfer characteristics for pressures of $10^{-2}$ Pa and $10^{-3}$ Pa are shown in Fig. 7.4. We extracted an onset voltage of 0.9 V and 1.2 V from the transfer curves. The measurement of the onset voltage is limited by the electrical setup. However, the error in determining the onset voltage is assumed to be small as the onset voltage can be extracted down to current levels of 10 pA. Furthermore, the oxygen exposure leads to an increase of the subthreshold slope from 0.2 V/decade to 0.4 V/decade. Such behavior is typical for polycrystalline pentacene thin film transistors characterized under ambient conditions [7.12, 7.15]. Numerical simulations indicate that the shift of the onset of the drain current is caused by acceptor-like states deep in the bandgap [7.16, 7.17]. The electrical in-situ measurements prove that the acceptor-like states are incorporated in the film by exposing the sample to oxygen. The two times sublimation purified source material (pentacene) is not the source of the impurities as no shift of the onset current is observed for the initial measurement. Furthermore, it can be excluded that the acceptor-like states are incorporated in the film during the organic molecular beam deposition of the pentacene film.

In the following the dopant concentration in the film was determined by analyzing the change of the subthreshold behaviour. The concentration of impurities in the pentacene film can be determined by analyzing the MOS structure of the organic TFT. A schematic cross section of a pentacene MOS structure and the corresponding electric and potential distributions are shown in Fig. 7.5. If the device operates in the linear region it can be assumed that the electric field in the channel is uniform, so that a uniform depletion layer is formed in the channel. Under such conditions the total potential ($V$) across the MOS structure is constant throughout the channel. The potential can be described the sum of the surface potential ($\phi_s$) and the potential across the dielectric ($V_0$), which it is given by [7.18]

$$V = q \cdot N_A \cdot W^2 + q \cdot N_A \cdot W \cdot d_{die} \cdot \frac{\varepsilon_o}{\varepsilon_o \cdot \varepsilon_{die}},$$  \hspace{1cm} (7.1)

where $d_{dep}$ is the width of the depletion layer, $N_A$ is the acceptor concentration in the film and $d_{die}$ is the thickness of the dielectric. $\varepsilon_{die}$ and $\varepsilon_{pen}$ are the relative permittivities of the dielectric and the pentacene film. $q$ is the elementary charge. The voltage $V$ is given by $V_G - V_{fb} - V_x$, where $V_G$ and $V_{fb}$ are the gate and threshold voltage. $V_x$ is the induced voltage during doping by impurities [7.18].

$$V_G - V_{fb} - V_x = q \cdot N_A \cdot \frac{W^2 \cdot \varepsilon_{die} + 2 \cdot W \cdot d_{die} \cdot \varepsilon_{pen}}{2 \cdot \varepsilon_o \cdot \varepsilon_{die} \cdot \varepsilon_{pen}}$$  \hspace{1cm} (7.2)

The voltage $V_x$ can be substituted by $V_G - V_{onset}$, where $V_{onset}$ is the onset voltage. The onset voltage is defined to be the voltage for which an increase of the drain current is observed. Furthermore, we assumed that the complete pentacene film is depleted.
Fig. 7.5: Schematic cross section of a pentacene Metal oxide semiconductor (MOS) structure and the corresponding space charge, electric and potential distribution.

Subsequently the following expression for the onset voltage can be derived.

\[
V_{\text{onset}} - V_{fb} = q \cdot d_{\text{pen}} \cdot N_A \cdot \frac{\varepsilon_{\text{die}} d_{\text{pen}} + 2 \varepsilon_{\text{pen}} d_{\text{die}}}{2 \varepsilon_0 \varepsilon_{\text{pen}} \varepsilon_{\text{die}}}.
\]  

(7.3)

As \( \varepsilon_{\text{die}} \cdot d_{\text{pen}} \) is much smaller than \( 2 \cdot \varepsilon_{\text{pen}} \cdot d_{\text{die}} \) the expression can be simplified in the following form

\[
V_{\text{onset}} - V_{fb} \approx \frac{q \cdot d_{\text{pen}}}{C_G} \cdot N_A,
\]

(7.4)

where \( C_G \) is the gate capacitance. The voltage \( V_{\text{onset}} - V_{fb} \) can be determined by comparing unexposed and exposed transistors. In this case the unexposed sample is used as a reference. Such approach was already suggested by Meijer and coworkers for polymer TFTs [7.5]. Based on the experimental results a minimum detectable concentration of acceptor-like states of \( 5 \cdot 10^{16} \text{ cm}^{-3} \) can be estimated. The transistor in Fig. 7.4 exhibits a concentration of acceptor-like states of \( 5 \cdot 10^{17} \text{ cm}^{-3} \). The calculated
concentration of acceptor-like states is in good agreement with numerical simulations of the electrical characteristic of pentacene TFTs [7.13]. The numerical model assumes a density-of-states model, which accounts for localized states. It is important to note, that the numerical simulation and the simple analytical model presented here do not account for the polycrystalline nature of the pentacene film. The model assumes a uniform distribution of acceptor-like states throughout the 10 nm thick film. Furthermore, it is assumed that the complete pentacene film is depleted. However, the defect states might be located at the pentacene grain boundaries. In these regions the pentacene film is thinner than 10 nm, so that the actual thickness of the depletion layer is overestimated. Accordingly the defect states might not be uniformly distributed throughout the film. Despite these restrictions Eq. (7.4) provides a good estimate of the concentration of acceptor-like states in the film. To calculate the precise concentration of acceptor-like states two-dimensional numerical device simulations have to be carried out [7.13,7.14] which take the polycrystalline nature of the film into account.

![Figure 7.6](image_url)

**Fig. 7.6:** Measured transfer characteristic of pentacene TFTs of different channel length at drain voltages of -1 V and -10 V. The transistors were exposed to dry oxygen before measuring the devices.

Further measurements of different device geometries indicate that the device structure and the formation of the pentacene film at the contacts have a strong influence on the electrical stability of the devices and the onset of the drain current. The transfer characteristics of different pentacene TFTs exposed to dry oxygen are shown in Fig. 7.6 for transistors with a channel length of 8 µm, 20 µm and 50 µm.

The onset voltage is shifted towards positive gate voltages with decreasing channel length. The transistors were exposed to oxygen for several hours (> 12 hours) before measuring the device characteristic. Transistor with a channel length of 8 µm exhibit a shift of the onset voltage by 6 V, whereas the shift of transistors with a channel length of
50 \mu m is only in the range of 0.5 V to 0.7 V. The results reveal that dry oxygen does not uniformly dope the pentacene films. Furthermore, it is known that the stability depends on the morphology and the structural properties of the organic films [7.7]. In order to study the morphology of the films Atomic Force Microscope (AFM) measurements were carried out.

An AFM image of a pentacene film is shown in Fig. 7.7. The image indicates that the film is highly ordered in the channel region of the transistor. The film exhibits the typical dendritic shape of highly ordered pentacene crystals [7.12]. Pentacene crystals with diameters exceeding 3 \mu m can be observed. However, the pentacene crystals close to the edge of the drain and source contacts are rather small and the density of grain boundaries is significantly increased. Similar morphologies have been observed for thiophene films on the same substrates [7.19].

Oxygen seems to be incorporated in the areas of low structural order. In order to account for the different structural properties of the pentacene film in the different parts of the channel, we modified Eq. (7.4). The acceptor defect density was substituted by \( N_A = \frac{L_C}{L} \cdot N_{contact} + \frac{(L-L_C)}{L} \cdot N_{channel} \), where \( N_{contact} \) and \( N_{channel} \) are the defect densities in the contact region and channel. \( L \) is the channel length and \( L_C \) is defined to be the contact region (Fig. 7.1), in which the density of grain boundaries is high. Substituting the acceptor concentration leads to the following expression:

\[
V_{onset} - V_{fb} \approx \frac{qd_{pen}}{C_G} \left[ \frac{L_C}{L} \cdot N_{contact} + \frac{L-L_C}{L} N_{channel} \right] \tag{7.5}
\]

If the concentration of acceptor-like states at the contact, \( N_{Contacts} \), is equal to the concentration of acceptor-like states in the channel, \( N_{channel} \), Eq. (7.5) is reduced to Eq. (7.4). The shift of the onset voltage and the subthreshold slope of the devices as a function of channel length are shown in Fig. 7.8 after exposing the sample to dry oxygen. The devices exhibit a strong shift of the onset as a function of the channel length. We used the AFM measurements (Fig. 7.7) to determine the width of the region.
close to the contacts, in which the grain boundary density is high. Describing the behaviour of the onset voltage in Fig. 7.8 by Eq. (7.5) reveals a defect density of $10^{19}$ cm$^{-3}$ in the vicinity of the contacts and a defect density of $1\cdot3\cdot10^{17}$ cm$^{-3}$ in the channel region. We assumed that the region of $L_C$ has a width of 1.5-2 µm. As the defect density at the contacts is much higher than the density in the channel, Eq. (7.5) can be approximated by

$$V_{onset} - V_{fb} \approx \frac{q_d}{C_G} \cdot \frac{L_C}{L} \cdot N_{contact} \cdot$$

(7.6)

Furthermore, the subthreshold slope of the devices is shown in Fig. 7.8. All devices exhibit subthreshold slopes in the range of 0.15 to 0.25 V/decade before being exposed to dry oxygen. Afterwards the subthreshold slope is increased due to the oxygen exposure. For the pentacene TFT with a channel length of 50 µm the sub threshold slope is only slightly increased to 0.18 V/decade. For the TFT with a channel length of 8 µm an increase of the subthreshold slope of up to 0.6 V/decade is observed. Therefore, the subthreshold slope is mainly determined by the onset of the drain current.

**Fig. 7.8:** Drain current onset (onset voltage – flatband voltage) and subthreshold slope as a function of the channel length for pentacene TFTs after oxygen exposure.

### 7.3.2 Influence of moisture on the device performance

In the following the influence of air plus moisture on the device characteristic of the transistor is investigated. Exposing the devices to air and moisture leads to a significant change of the transistor properties. Air plus moisture causes a drop of the charge carrier mobility and a shift of the drain current onset. Furthermore, the threshold voltage is slightly reduced, whereas the subthreshold slope remains almost the same. A comparison of a “fresh” sample (in-situ) and a transistor, which was exposed to air plus
moisture (ex-situ), is shown in Fig. 7.9. The transistor exhibits a channel length of 50 µm. The ex-situ measurement was taken after exposing the sample to air and moisture for 1 week. The transistor exhibits a charge carrier mobility of 0.25 cm²/Vs.

\[
I_D = \mu \cdot \frac{C_G \cdot W}{L} \cdot \left( V_G - V_T - \frac{V_D}{2} \right) \cdot V_D
\]

(7.7)

where \( W \) and \( L \) are the channel width and channel length of the TFT, respectively, \( C_G \) is the gate capacitance per unit area, \( V_G \), \( V_D \) and \( V_T \) are the gate voltage, the drain voltage and the threshold voltage. After exposing the sample to air and moisture for a one week the charge carrier mobility was reduced from 0.5 cm²/Vs to 0.25 cm²/Vs. The drop of the charge carrier mobility is caused by the influence of the drain and source contacts on the device performance.

The charge carrier mobility as function of the channel length and the inverse channel length is shown in Fig. 7.10. For transistors with a long channel (50 µm) a drop of the
charge carrier mobility by a factor of 2 is observed after exposing the device to air plus moisture.

![Graph](image)

**Fig. 7.10:** Charge carrier mobility as function of the channel length (left) and the inverse channel length (right) for pentacene TFTs. The transistors were measured in-situ, after exposing to dry oxygen and exposing to air plus moisture.

For TFTs with a shorter channel (5 µm) the charge carrier is reduced by a factor of 25. The fact that the drop of the charge carrier mobility is distinctly more pronounced for shorter channel devices reveals that the moisture does not only affect the electrical properties of the pentacene film in the channel region of the transistor. Otherwise the drop of the charge carrier mobility would be the same independent of the channel length. The distinct drop of the charge carrier mobility for shorter channel device indicates that moisture has an influence on the energy barrier at the metal/pentacene interface. The change of the energy barrier seems to be again closely related to the structural properties of the pentacene film in the vicinity of the drain and source contacts. The fact that pentacene TFTs with top drain and source contacts do not exhibit such strong drop of the mobility confirms this explanation.

The experimental results cannot be explained by an ohmic contact model, which was used in chapter 6. The channel length dependent data reveals that a schottky barrier is formed at the metal / pentacene interface. A schottky barrier is formed between the metal and the active layer interface when the work function of the metal does not coincide with the energy of the HOMO of the pentacene. The difference between the work function of the metal and energy of HOMO is also referred to as hole injection barrier, $\phi_h$ (see Fig. 7.11). Such a barrier results in non-linear (non ohmic) contact resistance. The barrier energy, $\phi_h$, depends on the metal / organic semiconductor. According to N. Koch et. al, the barrier energy, for gold / pentacene interfaces was determined to be 0.85 eV [20].
Another very important device parameter is the threshold voltage. The threshold voltage of the TFTs was reduced due to the exposure to moisture. The threshold voltage for TFTs with a 50 \( \mu \)m long channel was reduced from -5.2 V to -4.0 V. Transistors with a short channel lengths (8 \( \mu \)m) exhibit a reduction of the threshold voltage from -1.4 V to -1.0 V. In terms of the onset voltage and the subthreshold slope all devices exhibit a similar behaviour after exposing them to moisture. All transistors exhibit a subthreshold slope of 0.2 V/decade (±0.05 V/decade).

![Graph showing onset voltage vs. channel length](image)

**Fig. 7.11: Drain current onset (onset voltage – flatband voltage) and subthreshold slope as a function of the channel length for pentacene TFTs after exposure to air plus moisture.**
Therefore, the subthreshold slope is independent of the channel length. A similar behaviour was observed for the onset voltage. All transistors exhibit similar onset voltages. The onset voltage as a function of the channel length is shown in Fig. 7.11.

### 7.4 Discussion

The experimental results indicate that oxygen and moisture have different effects on the device characteristic of staggered pentacene TFTs. Oxygen leads to the creation of acceptor-like states, whereas the injection of charges in the channel of the transistor is not affected by oxygen as the charge carrier mobility and the threshold voltage is not changed. Furthermore, the channel length dependent shift of the onset voltage indicates that the acceptor-like states are formed in regions of reduced structural order. The non-uniform distribution of electronic defects in the film is supported by electric force microscopy measurements [7.21]. As the structural order is reduced close to the drain and source contacts the transistors exhibit a channel length dependent shift of the onset voltage.

The influence of oxygen on the electronic structure of the pentacene molecule is still not understood. However, ultraviolet photoelectron spectroscopy (UPS) studies of pentacene crystals and pentacene films on different substrates exhibit no change of the electronic structures of the pentacene molecules after oxygen exposure [7.22], whereas the electrical data presented in this manuscript provides clearly evidence for the formation of acceptor-like states. The electrical measurements are supported by first principle pseudopotential density function calculations. Such calculations indicate that the creation of -O or -OH defects lead to electronically active gap states [7.23]. In the case of oxygen such defect are located 0.18 eV and 0.62 eV relative to the valence band maximum. The energy required to form such a defect depends on the Fermi level, which might explain the difference between the ultraviolet photoelectron spectroscopy and the density function calculations. An applied gate voltage might be needed to modulate the Fermi level in order to create the defect states.

Exposing the device to air plus moisture leads to a change of several device parameters. The charge carrier mobility, the threshold voltage and the onset voltage are changed due to the influence moisture. The experimental results reveal that moisture has an influence on the metal/pentacene interface, so that the injection of charges in the channel is inhibited. Otherwise the distinct drop of the charge carrier mobility as a function of the channel length cannot be explained.

The analysis of the onset behaviour of the drain current according to Eq. (7.5) reveals a relatively low concentration of acceptor-like states close to the contacts, whereas the concentration of states in the channel region is high. A comparison between the two experiments in section 7.3.1 and 7.3.2 exhibit a rather different behaviour. Further investigations are needed to study the influence of moisture on the electronic properties of pentacene films and the metal / pentacene interface.

In order to realize complex electronic circuitry based on organic TFTs it is important that the device behaviour is stable and reproducible. As the devices are degraded by environmental conditions it is curial to develop strategies to minimize the creation of defects or to prevent the exposure of organic films to air and moisture. The formation of defect states can be reduced by using self-assembled monolayer (SAM) [7.1].
example the treatment of the gold electrode with thiol based self-assembled monolayers lead to a modified growth of pentacene film on the contact and in the vicinity of the contacts. Consequently the concentration of grain boundaries is reduced. This will lead to a reduced sensitivity towards oxygen and moisture. A detailed description of the contact treatment and the influence of these treatments on the device characteristic are given in chapter 8. Furthermore, effective encapsulation concepts are needed to minimize or inhibit the environmental degradation due to oxygen and moisture. The experiment results show that very efficient encapsulation concepts are needed as the device already exhibits a change of the device characteristic for low levels of oxygen.

7.5 Summary

The influence of environmental conditions on the electronic transport and the device operation of pentacene thin film transistors were investigated. Electrical in-situ and ex-situ measurements of pentacene TFTs were carried out to study the influence of oxygen and moisture on the device operation. Staggered TFT structures with bottom drain and source contacts were used for the device fabrication. Exposure of the pentacene film to dry oxygen leads to a shift of the onset of the drain current towards positive voltages due to the incorporation of acceptor-like states in the pentacene film. The charge carrier mobility and the threshold voltage are not affected by the oxygen contamination. The oxygen is incorporated in the film close to drain and source electrodes as the structural order of the pentacene film is reduced in this region of the device. A simple analytical model was presented, which correlates the shift of the onset voltage with the concentration of defect states in the film.

Exposing the devices to moisture causes a drop of the charge carrier mobility, a reduction of the threshold voltage and a shift of the onset voltage. The results indicate that moisture leads to the creation of acceptor-like states in the pentacene film, which is similar to the effect of oxygen on the device behaviour. Furthermore, the metal /organic interface at the drain and source electrodes are affected by the exposure of moisture as the injection of holes in the channel of the transistor is inhibited.

References

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8 Electrical Stability of Pentacene Thin Film Transistors

8.1 Introduction

The increasing interest in organic electronics can be attributed to the emerging demands in novel display media (active and passive) on low cost and/or flexible substrates. However, the realization of active matrix addressed displays or RFID tags require the fabrication of highly stable TFTs [8.1, 8.2]. In particular the threshold voltage has to be stable to allow for the realization of complex organic circuitry. Small variations of the threshold voltage might have a significant influence on the operation of displays or organic RFID tags. The change of the threshold voltage is usually caused by bias stress effects. Such effects occur for most thin film transistor fabricated at low temperatures. Bias stress effects have been observed for amorphous silicon [8.1, 8.3], polycrystalline silicon, organic [8.4-8.7] and polymeric TFTs [8.8,8.9]. To gain insights in the electronic transport and stability of polycrystalline pentacene TFTs electrical in-situ and ex-situ measurements were carried out. The influence of environmental conditions and its effect on electrical stability and device operation was studied by exposing the TFTs to dry oxygen and moisture.

The influence of threshold variations on the operation of organic integrated circuits is described in section 8.2. The fabrication of the pentacene TFTs will be described in section 8.3 of the chapter. The experimental results will be presented in section 8.4, which is divided in four subsections. In the first subsection, 8.4.1, the electrical characteristic of pentacene TFTs under ambient conditions will be described. Electrical measurements of pentacene transistors under different bias stress conditions will be described in section 8.4.2. In section 8.4.3 the influence of contacts on the operation of organic transistors will be investigated. The influence of electrical bias stress on the device operation of organic circuits like pixel drivers for organic light emitting diode (OLED) displays will be described in section 8.4.4. Influence of electronic defects or environment on the electrical stability, and the different strategies how to minimize the influence of environmental conditions on the device operation will be discussed in section 8.5. Finally, the chapter will be summarized in section 8.6.

8.2 Influence of bias stress on the performance of organic circuits

The influence of bias stress on the performance of organic integrated circuits will be investigated in the first section of this chapter. As an example the influence of bias stress on the operation of an organic light emitting (OLED) pixel driver will be described. A simple two-transistor (2T) OLED pixel circuit is shown in Fig. 8.1 [8.10]. The pixel circuit comprises of a select transistor, $T_s$, which transfers the input signal (charge) from the external drive electronics to the storage capacitor in the pixel. The charged on the storage capacitor, $C$, is used to bias the drive transistor $T_D$. It is assumed that the drive transistors can be described by the classical transistor equation

$$I_D = k \cdot \frac{W}{L} \cdot \mu \cdot C_G \cdot (V_G - V_T)^m$$  \hspace{1cm} (8.1)
where $\mu$ is the mobility, $W$ and $L$ are the channel width and length. If the drain voltage, $V_D$, is smaller than $V_G - V_T$ the parameter $m$ is equal 1 and the TFT operates in the linear region. Under such conditions the prefactor $k$ is equal to $V_D$. If the drain voltage $V_D \geq V_G - V_T$ the transistor operates in the saturation region. Subsequently the parameter $m$ is equal 2 and the prefactor $k$ is equal to $\frac{1}{2}$.

In the following the transistor operates as a drive transistor in an organic pixel circuit [8.10]. It was assumed that a certain drain current variation ($\Delta I_D/I_D$) can be tolerated without having a negative effect on the image quality of the display. Thus the following relationship between the threshold voltage shift and the variation of the drain current can be derived:

$$\Delta V_T = -(V_G - V_T) \cdot \frac{\Delta I_D}{m \cdot I_D}.$$  
(8.2)

The parameter $m$ is equal 1 in the linear and equal to 2 in the saturation region. In the saturation mode of operation it can be assumed that $V_G - V_T$ is small, for example, $V_G - V_T$ is equal to -1V. If a variation of the drain current by 10% can be tolerated by the display, a maximum variation of the threshold voltage by 50 mV can be determined. In the linear region of operation the term $V_G - V_T$ is going to be larger, for example -5V. Subsequently a threshold voltage variation of 500 mV can be tolerated by the display. In general, the requirements in terms of the threshold voltage stability are high in the saturation region, whereas the requirements in the linear region are distinctly lower. Therefore, a variation of the threshold voltage by 500 mV in the linear region of operation defines the minimum requirement in terms of the threshold voltage stability.

![Fig. 8.1: Circuit of an organic light emitting diode (OLED) pixel using a two-transistor configuration.](image)

### 8.3 Fabrication of organic thin film transistors

The pentacene thin film transistors (TFT) were fabricated as described in section 7.2. A
highly doped silicon wafer was used as a substrate. The gate dielectric of the transistor was formed by a 50 nm thick silicon oxide layer. Bottom drain and source contacts were defined by optical lithography. The pentacene layer has a thickness of 10-15 nm. The channel length of the device ranges from 5 to 150 µm. To improve the device performance of the TFTs, the dielectrics were treated by hexamethyldisilazane (HMDS) prior to the deposition of the pentacene film. Self-assembled monolayers (SAMs) like HMDS change the surface wetting properties of the dielectric and the growth of the organic film. A detailed description of the preparation of self-assembled monolayers and the influence of the SAMs on the device performance of organic thin film transistors is given in Ref. 8.18.

### 8.4 Pentacene TFTs under ambient conditions

![Transistor Characteristics](image)

**Fig. 8.2**: Transfer characteristic of a pentacene TFT measured under ambient conditions (ex-situ measurement). The transistor has a channel length of 20 µm and a W/L ratio of 10000.

The transfer characteristics of a pentacene TFT with a channel length of 20 µm and a width to length ratio (W/L) of 10,000 is shown in Fig. 8.2. The transistor was measured under ambient conditions. The pentacene film has a thickness of 10 nm. The pentacene
film was prepared on top of an HMDS treated thermal oxide gate dielectric with a thickness of 50 nm. The transistors exhibit a charge carrier mobility of 0.4-0.6 cm$^2$/Vs, a threshold voltage of -2.0 V and an on/off ratio of more than 8 orders of magnitude. Furthermore, the transistor exhibits a pronounced subthreshold region and a positive onset of the drain current. Such behaviour is typical for polycrystalline pentacene TFTs characterized under ambient conditions [8.4-8.9,8.10-8.13]. Numerical simulations of the electrical transistor characteristic indicate that the shift of the onset of the drain current is caused by acceptorlike states deep in the band gap [8.6,8.11,8.14,8.15]. The acceptors like states are supposed to be created by oxygen or –OH molecules that are incorporated in the organic film [8.16, 8.17].

8.5 Influence of bias stress on pentacene thin film transistors

Stable transistor operation is essential for the realization of organic integrated circuits. In particular, variations of the threshold voltage have a distinct influence on the operation of OLED displays or organic radio frequency identification tags (RFID). Major sources of instabilities are bias stress effects, which leads to a change of the threshold voltage over time. Such effects are well known for inorganic and organic TFTs prepared at low temperatures. The threshold voltage shift for amorphous and polycrystalline silicon TFTs has been extensively investigated [8.1,8.2]. The effect can arise from slow trapping in the dielectric and/or surface states at the semiconductor/dielectric interface, or defect creation in the semiconductor. So far, few studies have been published addressing these issues in organic thin film transistors [8.4-8.6,8.8-8.10].

Bias stress effects are closely related to the electronic structure of the organic films. The electronic structure is again related to impurities in the film, which are affected by environmental conditions. Therefore, it can be expected that environmental conditions have a strong effect on the stability of organic thin film transistors.

To avoid the influence of environmental conditions on the device behavior the bias stress experiments were carried out under high vacuum conditions ($\sim 10^6$ Pa). The transfer characteristics of a pentacene TFT with a channel length of 40 and 140 µm with a width of 4,000 µm is shown in Fig. 8.3. The samples exhibits a hole mobility of 0.2-0.6 cm$^2$/Vs and a subthreshold slope of $\sim$ 0.2 V/decade using a 50 nm thick silicon oxide gate dielectric. After measuring the initial transfer and output characteristics (0 min, unstressed device) the pentacene transistors were stressed for 10min, 30min, 90min and 180min at different gate and drain voltages. Afterwards, regular measurements of the I/V curves were carried out. Interestingly, no change of the device characteristic was observed after stressing the devices up to 180 min.

The bias stress experiment was repeated after exposing the devices to dry oxygen. The concentration of dry oxygen in the system was controlled by the pressure in the high vacuum chamber. The transfer characteristic of a pentacene TFT after exposure to oxygen (before applying bias stress) is shown in Fig. 8.3. The oxygen exposure results in a shift of the onset of the drain current towards positive gate voltages. The charge carrier mobility and the threshold voltage of the transistors were not affected by the oxygen contamination. The onset voltage was shifted by 1 and 3.2 V for a channel length of 140 and 40 µm. Furthermore, the oxygen exposure leads to a slight increase.
of the subthreshold slope. The shift of the drain current onset is caused by acceptorlike states deep in the band gap [8.6,8.9,8.12,8.13].

As mentioned in chapter 7, the concentration of acceptorlike states in the film can be determined by analyzing the MOS structure of the pentacene transistor. The voltage applied to the MOS structure is equal to \( V = V_0 + \varphi_S \), where \( V_0 \) is the voltage drop across the dielectric and \( \varphi_S \) corresponds to the band bending at the interface (surface potential) due to the influence of the impurities. The voltage drop across the dielectric and the surface potential can be determined by the classical theory for Metal Oxide Semiconductor (MOS) structures [8.16]. By analyzing the band bending of the semiconductor the doping concentration can be determined by,

\[
N_A = \frac{C_G}{d_{pen}} \cdot \frac{V_{onset} - V_{fb}}{q},
\]

(8.3)

where \( C_G \) is the gate capacitance, which is calculated by \( C_G = \varepsilon_0 \cdot \varepsilon_{die}/d_{die} \). \( \varepsilon_0 \cdot \varepsilon_{pen} \) and \( \varepsilon_0 \cdot \varepsilon_{die} \) are the permittivity of the pentacene film and the gate dielectric, \( d_{pen} \) and \( d_{die} \) are the thicknesses of the pentacene film and the gate dielectric. \( q \) is the elementary charge. Eq. (8.3) is valid if the complete organic film is depleted. The voltage \( V_{onset} - V_{fb} \) can be determined by comparing unexposed and exposed transistors. The unexposed sample is used as a reference to determine the flat-band voltage. Such approach was
already suggested by Meijer et al. [8.17] for polymer TFTs and Knipp et al. [8.18] for small molecule based TFTs. Based on the experimental results an acceptor concentration of $5 \cdot 10^{17} \text{cm}^{-3}$ was estimated for a transistor with a channel length of 140 $\mu\text{m}$ and a concentration of $1.5 \cdot 10^{18} \text{cm}^{-3}$ was estimated for a transistor with a channel length of 40 $\mu\text{m}$.

After exposing the device to oxygen the devices were stressed for 10 min, 30 min, 90 min, and 180 min. The transfer characteristics after stressing the transistor in the on-state are shown in Fig. 8.3. The drain voltage was kept constant at -10 V and the gate voltage was fixed at $V_G = -20$ V. Due to bias stress the transfer curves were shifted towards negative gate voltages. The charge carrier mobility, the on/off ratio and the subthreshold slope of the transistor are not affected by the bias stress experiment. The bias stress results in a threshold voltage shift of 0.7 V towards negative gate voltages. The opposite behavior is observed if the transistor is bias stressed in the off-state (positive gate voltage). As a consequence the threshold voltage shifts towards positive gate voltage. The data in Fig. 8.3 represents typical bias stress data. The devices were stressed several times in the on- and the off-state before extracting the shift of the threshold voltage from the transfer characteristic.

Fig. 8.4: Measured transfer curve of a pentacene TFT with a channel length of 40 $\mu\text{m}$ after applying bias stress to the device. The transfer curves were measured after 0 min, 10 min, 30 min, 90 min and 180 min of prolonged bias stress. The transistor was stressed in the on-state. The drain voltage and gate voltages were kept constant at -10 V and -20 V during the bias stress experiment.
A summary of the bias stress experiment for different transistors under positive and negative bias is given in Fig. 8.5. The shift of the threshold voltage is plotted as a function of time (linear (Fig. 8.5a) and logarithmic time scale (Fig. 8.5b). Fig. 8.5a and 5b show the shift of the threshold voltage for pentacene TFTs with a channel length of 40 \( \mu m \), 115 \( \mu m \) and 140 \( \mu m \). All devices have the same channel width of 4000 \( \mu m \). We observed that the shift of the threshold voltage due to bias stress is channel length dependent. The shift is more pronounced for TFTs which shorter channels.

The shift of the threshold voltage as a function of time can be described by the following stretching exponential model \([8.10, 8.19]\), which is typically used to describe bias stress effects in amorphous silicon TFTs,

\[
\Delta V_T \propto (V_G - V_T) \left( 1 - \exp \left( -\left( \frac{t}{\tau} \right)^\gamma \right) \right)
\]

(8.4)

where \( t \) corresponds to the stress time, and \( \gamma \) is a stretching factor. The time constant \( \tau \) depends on the material and device parameters. The shift of the threshold voltage is described very well by Eq. (8.4). The marks in Fig. 8.5a and 8.5b represent the experimental data, whereas the solid lines correspond to the fit of the data. For positive gate bias the stretching factor increases with increasing channel length from \( \gamma = 0.7 \) to 0.85. The opposite behavior is observed for the time constant \( \tau \), which decreases with increasing channel length from \( \tau = 540 \) s to 360 s. For negative bias stress and increasing channel length the stretching factor \( \gamma \) increases from 0.32 to 0.40. For negative voltages the time constant, \( \tau \), is 100 to 1000 times higher than the time constant for positive bias voltages.

Other models including power law models have been proposed in literature in order to account for the threshold voltage shift upon prolonged bias stress \([8.10]\). However, the experimental data in Fig. 8.5 can only be described by the stretching exponential model. For positive bias stress the threshold voltage converges towards an upper bound. Only the stretching exponential model accounts for such behavior. The situation is different for negative gate bias stress. Here the experimental data does not show a lower bound.

The experimental results reveal that electronic defects are created during the oxygen exposure of the device. During the bias stress experiment, which was carried out under vacuum conditions, the defect states are charged or recharged, but no additional defects are created. Subsequently the threshold voltage converges towards an upper bound for positive bias stress. Further measurements have to be carried out for negative bias stress. It remains open whether a lower bound for the threshold voltage exists.

Measurements under different biasing conditions show that the shift of the threshold voltage increases with increasing bias stress applied to the gate and the drain electrodes. Similar experiments carried out under ambient conditions (oxygen plus moisture exposure) exhibit a more pronounced shift of the threshold voltage \([8.10]\). However, the fundamental trend remains the same. The threshold voltage shifts towards positive (negative) gate voltages, if the device is stressed at positive (negative) gate voltages \([8.10]\). However, bias stress experiments carried out under ambient conditions do not exhibit an upper bound for the threshold voltage, which reveals that electronic
defects are charged or recharged and new defects are created during the stress experiment [8.10].

After stressing the devices for 180 min. and characterizing the samples the gate and drain electrodes were grounded. The transfer curves of the TFT were measured periodically over a period of days to obtain the threshold voltage. Measurements show that the threshold voltage of the transistor recovers. The threshold voltages shifts back towards the threshold voltage, which was obtained after exposing the sample to dry oxygen. However, further measurements are needed to study long-term bias stress effects. Recent investigations of polymer TFTs shows that it is necessary to distinguish between permanent and reversible shifts of the threshold voltage [8.20,8.21].

![Graph showing threshold voltage shift vs time for different channel length](image)

**Fig. 8.5:** Measured shift of the threshold voltage of pentacene TFTs for different channel length after applying bias stress. The devices were exposed to oxygen before carrying out the bias stress experiment.

### 8.6 Influence of contacts on the electrical stability of pentacene transistors

The electrical stability of organic transistors is influenced by the structural properties of the organic film. Pentacene films with increased structural order are less susceptible to bias stress and environmental influences. Therefore, staggered transistors using bottom drain and source electrodes are less stable than thin film transistors with top drain and source electrodes. The pentacene film close to the contacts of the bottom drains and
source transistors exhibit an increased structural disorder so that the overall stability is reduced [8.20].

![Diagram of staggered pentacene transistor](image)

**Fig. 8.6:** Schematic cross section of a staggered pentacene transistor with bottom drain and source contacts. The bottom drain and source contacts (gold) were treated by eicosanethiol and the gate dielectric (silicon oxide) by hexamethyldisilazane self-assembled monolayer (SAM) prior to the deposition of the pentacene film.

![Atomic force microscope images](image)

**Fig. 8.7:** Atomic force microscope images of pentacene films prepared on silicon oxide dielectrics and gold drain/source electrodes. The gate dielectric was treated by a hexamethyldisilazane self-assembled monolayer (SAM) prior to the deposition of the pentacene film. In the contact region the pentacene was prepared on pure gold drain/source electrodes (a) and gold electrodes treated by 2-Mercapto-5-nitrobenzimidazole (MNB) (b).
In the case of bottom drain and source contacts the structural order of organic films can be increased by modifying the surface property of the contacts and/or the channel region by self-assembled monolayers (SAMs). The gold electrodes can be treated by using eicosanethiol, hexadecanethiol, 2-Mercapto-5-nitrobenzimidazole, thiophenol, or 4-nitrothiophenol self-assembled monolayers prior to the deposition of the pentacene film. All these SAMs comprise of –SH (thiol) head groups, which bond to the gold surface. Subsequently the growth of pentacene on the metal electrodes and close to the metal electrodes is improved.

Fig. 8.6 shows a schematic cross section of a device structure, which was treated by self-assembled monolayers. The silicon oxide dielectric was treated by hexamethyldisilazane (HMDS), whereas the gold electrodes were treated by 2-Mercapto-5-nitrobenzimidazole (MNB). The corresponding atomic force microscope image is shown in Fig. 8.7b. The pentacene film was prepared according to the deposition conditions described in section 2.

Fig. 8.7: Transfer characteristic of pentacene thin film transistors prepared on a silicon oxide dielectric with bottom drain and source electrodes. The pentacene films were prepared on pure gold and 2-Mercapto-5-nitrobenzimidazole (MNB) pretreated gold drain and source electrodes.

The pentacene film is highly ordered in the channel and the contact region. Pentacene films on pure gold surfaces are disorder and the pentacene molecules are lying flat on the gold surfaces. An atomic force microscope image of a pentacene film prepared on a pure gold electrode is shown in Fig. 8.7a. The pentacene film has a thickness of 10 nm. The channel region was treated by HMDS, whereas the gold electrode was untreated.
A comparison of the transfer characteristic of transistors with treated and non-treated bottom drain and source electrodes are shown in Fig. 8.8. The channel of the transistors is 20 µm long. Both devices were exposed to dry oxygen before measuring the transistor. Only the device with untreated gold electrodes exhibits a shift of the onset voltage due to the oxygen exposure. The onset voltage of the transistor with pretreated bottom and source electrodes does not exhibit a change of the onset voltage due to the oxygen exposure. Furthermore, the SAM treatment has an influence on the threshold voltage. The threshold voltage of the transistors with untreated drain and source electrodes is higher. The charge carrier mobility of pentacene TFTs with treated drain and source electrodes is increased in comparison to transistors with treated electrodes. In particular short channel transistors exhibit a distinct increase of the charge carrier mobility by 30-50%.

8.7 Discussion

The electrical stability of organic thin film transistors is a very important requirement for the realization of organic integrated circuits and display applications. In particular the stability of the threshold voltage is of major importance for the realization of organic integrated circuits. In general the change of the threshold voltage due to bias stress is caused by charge trapping or recharging of defect states in the dielectric, trapping and slow release of carriers in existing deep states in the semiconductor (bulk or interface), or a reversible structural change in the semiconductor that creates new traps. The fact that bias stress is only observed after exposing a pentacene TFT to dry oxygen indicates that trapping of charges in the dielectric can be excluded as a source of the threshold voltage shift. The results reveal that recharging of electronic defects in the channel material causes the threshold voltage shift. In order to account for the shift of the threshold voltage in Fig. 8.5a defect density of more than $1.5 \times 10^{17}$ cm$^{-3}$ is required.

Furthermore, the defects need to be acceptorlike for positive bias stress and donorlike for negative bias stress. First principle pseudopotential density function calculations of -O and -OH defects in pentacene shows that such impurities lead to the creation of electronically active gap states [8.15]. In the case of oxygen such defect are located 0.18 eV (donorlike states) and 0.62 eV (acceptorlike states) relative to the valence band maximum. Further electrical measurements including temperature dependent electronic transport measurements and/or numerical simulations are needed to determine the energy level and the concentration of the defect states.

A comparison of the experimental results presented in this chapter with other results published in literature indicates that the shift of the threshold voltage due to bias stress is relatively small [8.1,8.3-8.8,8.8, 8.10]. However, the shift of the threshold voltage does not fulfill the requirements defined for a drive transistor in an OLED display. The shift of the threshold voltage due to bias stress exceeds the required limits in the linear and the saturation mode of operation. As the actual bias stress induced shift of the threshold voltage (Eq. (8.2)) and the maximum tolerable threshold voltage shift (Eq. (8.4)) scale with $V_G-V_T$ further aspects have to be taken into account when deciding on the mode of operation of the drive transistor. It should be mentioned that the requirements in terms of OLED pixel circuits are very high. Polycrystalline silicon TFTs are typically used as pixel circuits as the devices are very stable.
In terms of other displays like active matrix addressed liquid crystal (AMLCD) displays or reflective displays the requirements are not as high. For such applications the stability of pentacene TFTs is sufficient [8.22]. Preliminary bias stress measurements carried out under vacuum conditions (no oxygen exposure) do not exhibit a change of the device characteristic upon prolonged bias stress (180 min.). These results underline the importance of effective encapsulation concepts, which prevent the exposure to oxygen and moisture. However, the experimental results show that very efficient encapsulation concepts are needed, as the device already exhibit distinct changes of the device characteristics for rather low levels of oxygen.

8.8 Summary

The influence of environmental conditions on the device operation and the electrical stability of staggered polycrystalline pentacene thin film transistors (TFTs) with bottom drain and source contacts were investigated. In-situ and ex-situ measurements of pentacene TFTs were carried out to study the effect of oxygen contamination on the operation and the stability of pentacene TFTs. Oxygen exposure leads to a shift of onset of the drain current towards positive gate voltage. The experimental results show a clear correlation between the shift of the onset voltage and the electrical stability of the devices. A shift of the onset voltage upon oxygen exposure is correlated with a shift of the threshold voltage upon prolonged bias stress. The shift of the threshold voltage upon prolonged bias stress is larger for short channel devices, whereas long channel devices exhibit a small shift of the threshold voltage upon prolonged bias stress. Applying self-assembled monolayers can help to reduce the sensitivity towards oxygen and therefore, the bias stress induced shift of the threshold voltage.

The example of a pixel driver of an organic light emitting display was investigated in terms of the required device stability. A simple relationship between the acceptable variation of the drive current and the maximum shift of the threshold voltage was derived. The simple estimation reveals that efficient encapsulation concepts are needed to use pentacene TFTs in complex organic integrated circuits. Measurements under vacuum conditions do not show bias stress induced changes of the threshold voltage, which underlines the huge potential of organic transistors for a variety of applications.

References

9 Summary

Flexible, lightweight, large area electronics realized by low cost approaches has gained considerable attention in recent years. Research is initiated by the large interest and demand in electronic devices like large area display, smart cards and radio frequency identification tags (RFID). Such electronic device can only be realized at low cost if novel materials and material systems and new ways of fabricating devices and systems are developed. Organic semiconductors are a very promising material system used for such applications. Organic materials and organic devices can be printed, which allows for large area processing at low fabrication cost.

In the first part of the thesis different patterning methods based on microcontact printing were developed. Microcontact printing allows for the fast patterning of micro and nano structures over relatively large areas and flexible substrate at low cost. During the printing process an elastomeric stamp is brought in conformal contact with the surface and the molecules are transferred directly to the surface where they form a self-assembled monolayer (SAMs).

Silane based self-assembled monolayers as wetting agent:

The first patterning method is based on microcontact printed self-assembled monolayers in combination with selective dewetting of polymer/resist. The process provides a simple route in patterning metals, semiconductors, and insulators on substrate such as glass and silicon. Self-assembled monolayers such as OTS (octadeyltrichlorosilane) were microcontact-printed on glass or silicon substrates. The patterned OTS film leads to the formation of hydrophilic and hydrophobic regions on the substrate. Such functionalized substrates facilitate selective wetting of surfaces by polymers or resists. The approach was used to pattern metal electrodes by a lift-off process. Radio-frequency microcoils, interconnects, and electrodes for transistors were realized by this approach. The resolution of the patterning process is determined by the selective dewetting of polymers and not by the microcontact printing of the SAMs. The resolution of the selective dewetting process depends on several parameters, including the surface tension of the substrate and viscosity of the polymer. A resolution of 2 µm was achieved for parallel electrodes using a combination of microcontact printing of OTS and selective dewetting of PMMA (polymethyl methacrylate). Furthermore, the achieved resolution depends on the geometry of the printed structures. Fundamentally, the resolution of the selective-wetting process is limited by the surface tension of the substrate and viscosity of the polymer, which again depends on the polymer type, solubility of the polymer, and intermolecular forces between the polymer chains and solvents.

Thiol based self-assembled monolayers as etch resist:

Thiol based SAMs can be used as etch masks to pattern thin metallic films like gold, silver or copper. In this study, silver and gold films were patterned over flexible and rigid substrates using alkyl thiol SAMs as etch resist and ferri/ferrocyanide as etchant. The patterning process was systematically investigated in terms of the etching window and the etching selectivity. The study has showed that the etch rate of the ferri/ferrocyanide
etching solution is higher for silver than for gold. The maximal film thickness, which can be patterned by the process, depends on the etching selectivity of the process. A comparison of gold and silver shows that the selectivity is higher for silver resulting in a larger relative etching window for silver. Silver films with a thickness of up to 300nm were patterned by this approach.

Thiol based self-assembled monolayers as wetting agent:
The second alternative printing method is based in using alky thiol SAMs as wetting agent. The alkyl thiol printed regions are hydrophobic, while the unprinted regions stay hydrophilic, so that resists like PMMA can be selectively deposited in the hydrophilic regions of the prepatterned substrate, whereas the hydrophobic regions stay uncoated. Subsequently, the patterned polymer is used as etch resist to pattern gold and silver films by a KI/I₂ (potassium iodide/iodine) etching solution. The method allows to pattern gold and silver films over flexible foil, glass and silicon. The method is relatively environmental friendly and compatible with existing processes in standard semiconductor processing.

In the second part of the thesis the different patterning methods where used to pattern electrodes of organic thin film transistors.

Organic thin film transistors with printed electrodes:
Next, pentacene thin film transistors with printed drain/source electrodes were fabricated and characterized. The drain/source electrodes were realized by microcontact printing in combination with a lift-off process and wet chemical etchings. Pentacene TFTs fabricated by printing and wet etching exhibit charge carrier mobilities comparable to TFTs fabricated by photolithography. A simple transistor model was used to study the influence of the different printing techniques on the transistors properties. The transistors fabricated by microcontact printing and lift-off process exhibit an increased contact resistance, which leads to a reduction of the effective charge carrier mobility. The experimental results reveal that the contact resistance depends on the fabrication method of the electrodes. The contact resistance of TFT fabricated by printing and a lift-off is increased due to the formation of a burr-like structure at the edge of the electrodes, which limits the injection of charges in the channel of the transistor.

In the third part of the thesis the influence of environmental conditions on the electronic transport and the electrical stability of pentacene thin film transistors were investigated.

Environmental stability of pentacene thin film transistors:
The influence of environmental conditions on the electronic transport and the device operation of pentacene thin film transistors was investigated. Electrical in-situ and ex-situ measurements of pentacene TFTs were carried out to study the influence of oxygen and moisture on the device operation. Staggered TFT structures with bottom drain and source contacts were used for the device fabrication. Exposure of the pentacene film to dry oxygen leads to a shift of the onset of the drain current. The drain current shifts towards positive voltages due to the incorporation of acceptor-like states in the
pentacene film. The charge carrier mobility and the threshold voltage are not affected by the oxygen contamination. The oxygen is incorporated in the film close to drain and source electrodes as the structural order of the pentacene film is reduced in this region of the device. A simple analytical model was presented, which correlates the shift of the onset voltage with the concentration of defect states in the film. On the other hand, exposing the devices to moisture causes a drop of the charge carrier mobility, a reduction of the threshold voltage and a shift of the onset voltage. The results indicate that moisture leads to the creation of acceptor-like states in the pentacene film, which is similar to the effect of oxygen on the device behavior. Furthermore, it has been proved that the metal/organic interface at the drain and source electrodes are affected by the exposure of moisture and results in poor injection of holes in the channel of the transistor.

**Electrical stability of pentacene thin film transistors:**

Next, the electrical stability of pentacene TFTs was studied. The charge carrier mobility, the on/off ratio and the subthreshold slope of the transistor are not affected by the bias stress experiments. Electrical bias stress studies showed that a shift of the onset voltage upon oxygen exposure is correlated with a shift of the threshold voltage upon prolonged bias stress. The shift of the threshold voltage upon prolonged bias stress is larger for short channel devices, whereas long channel devices exhibit a small shift of the threshold voltage upon prolonged bias stress. Furthermore, it was observed that applying self-assembled monolayers could help to reduce the sensitivity towards oxygen and therefore, the bias stress induced shift of the threshold voltage. More importantly, it was found that prolonged bias stress under vacuum conditions does not lead to a change of the threshold voltage, which underlines the huge potential application of organic transistors for different of applications.

The results underline the importance of effective encapsulation concepts, which prevent the exposure to oxygen and moisture. However, the experimental results show that very efficient encapsulation concepts are needed since the device already exhibit distinct changes of the device characteristics for rather low levels of oxygen. In order to prevent or minimize the influence of oxygen and moisture on the device performance new fabrication or encapsulation concepts have to be developed.
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Publications and Conference Presentations

Publications


Conference presentations


